

FIG. 1

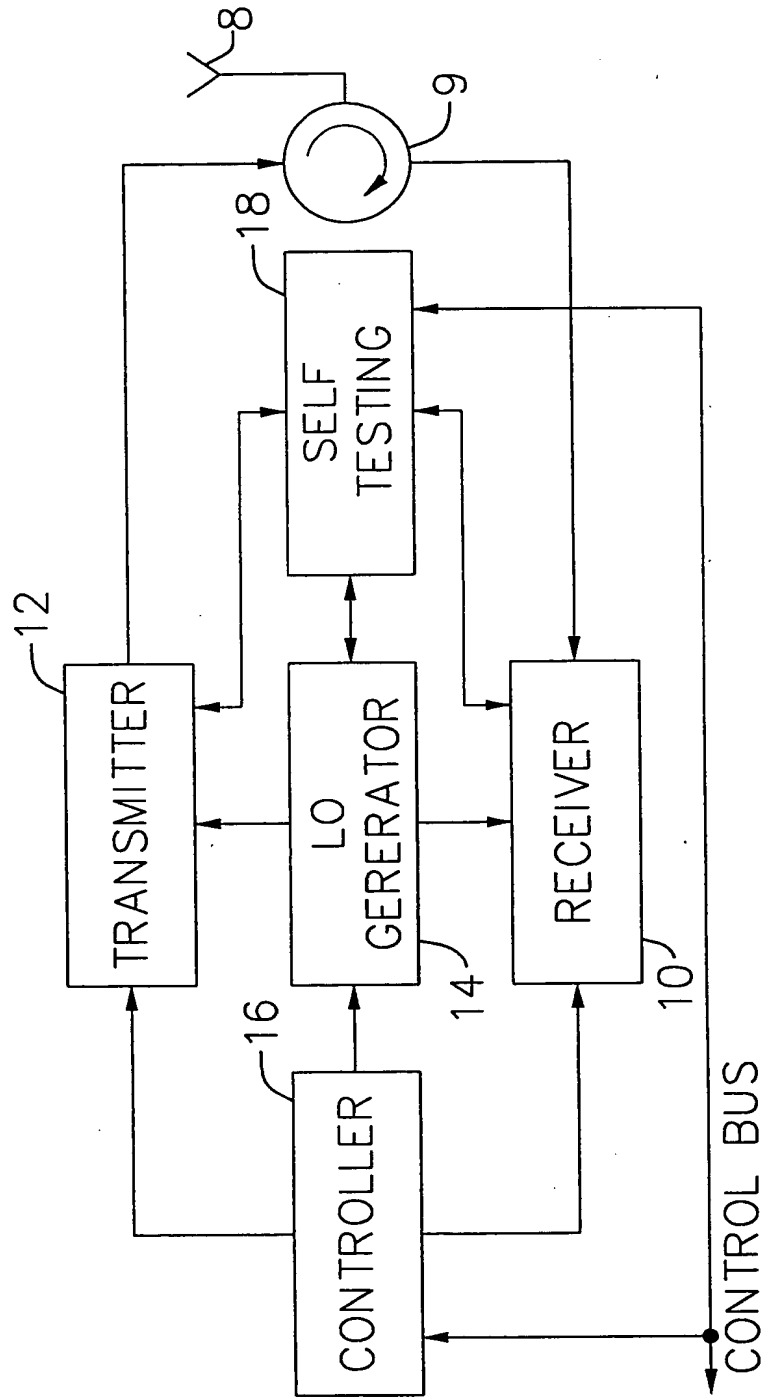
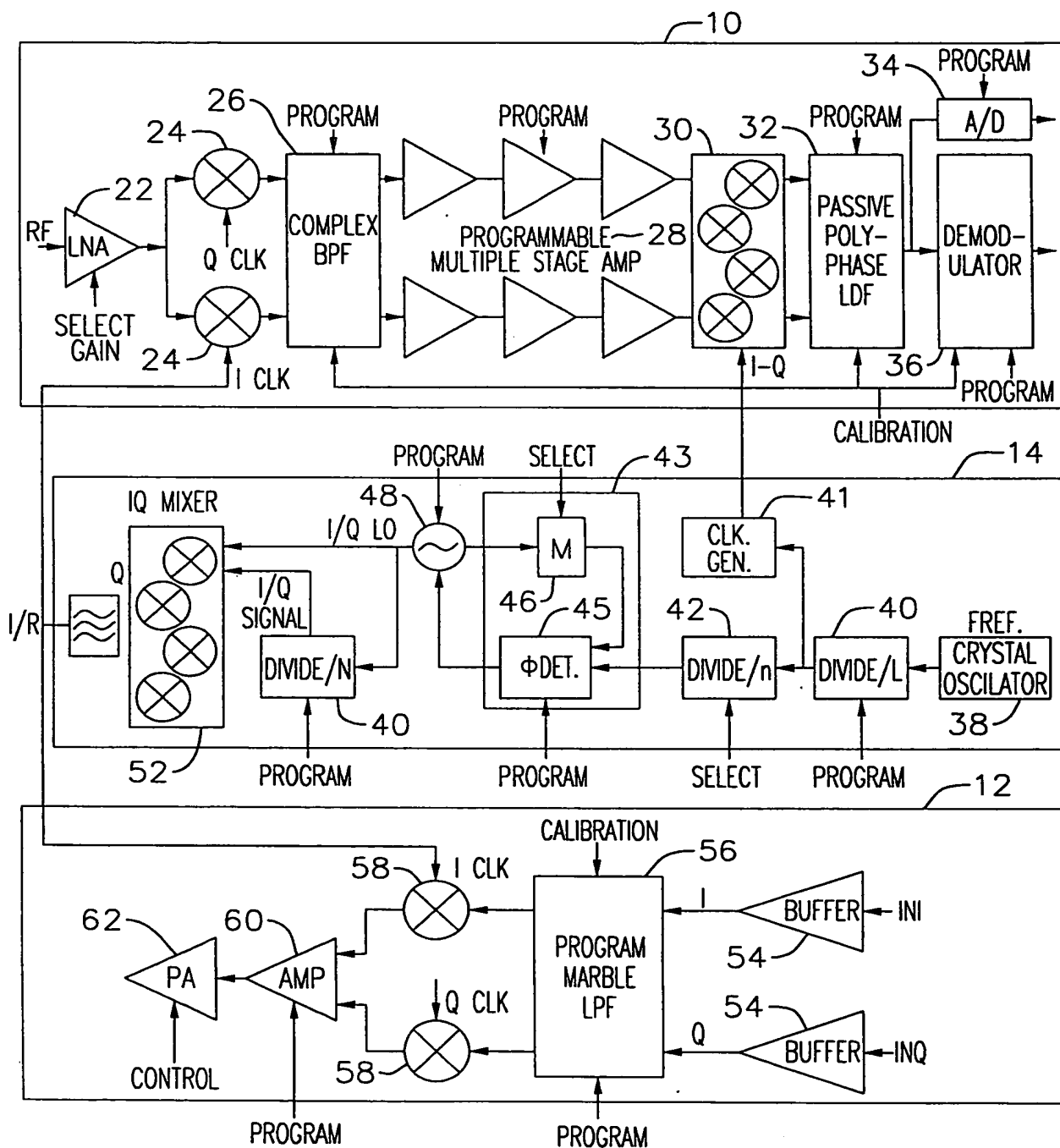
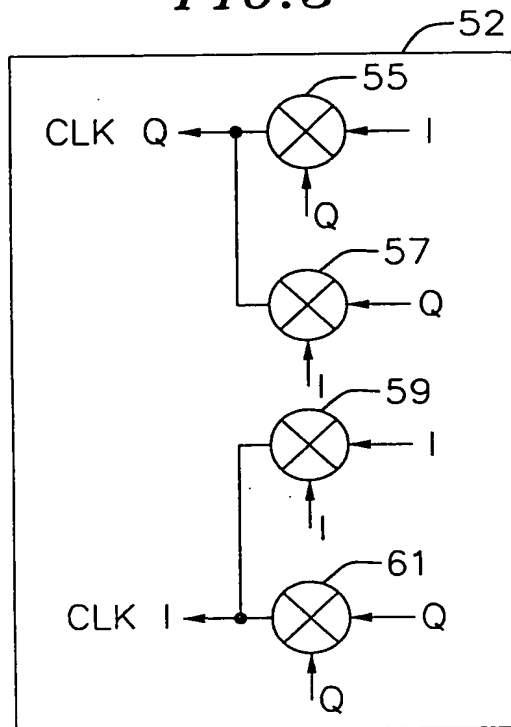


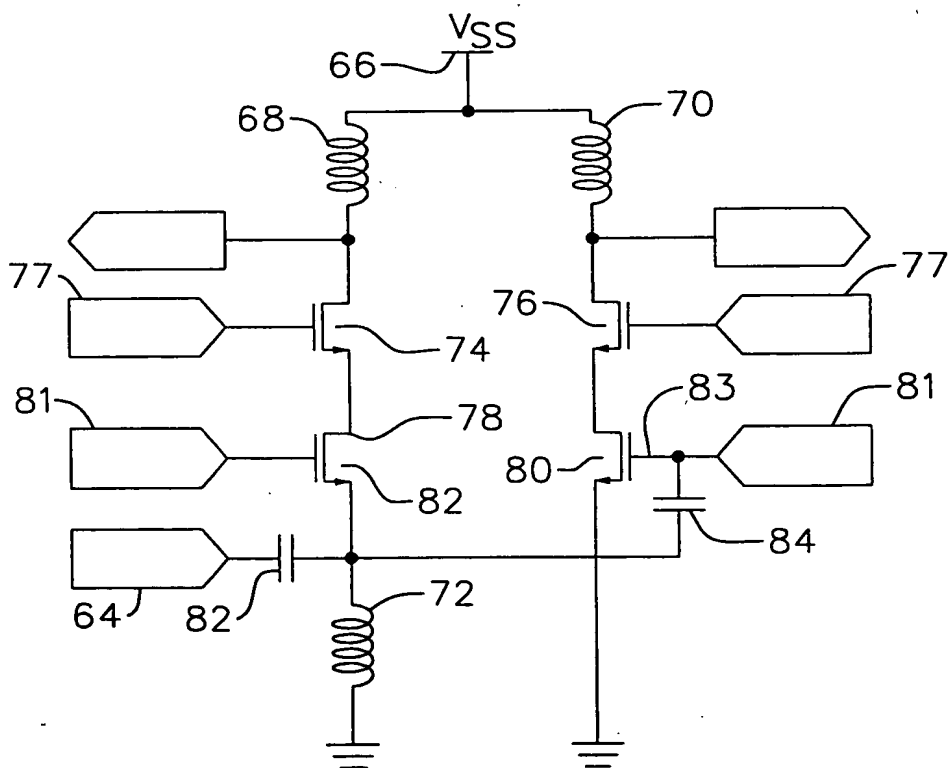
FIG. 2



*FIG. 3*



*FIG. 4*



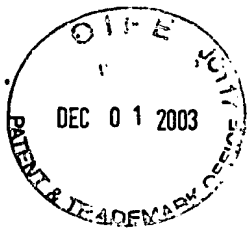
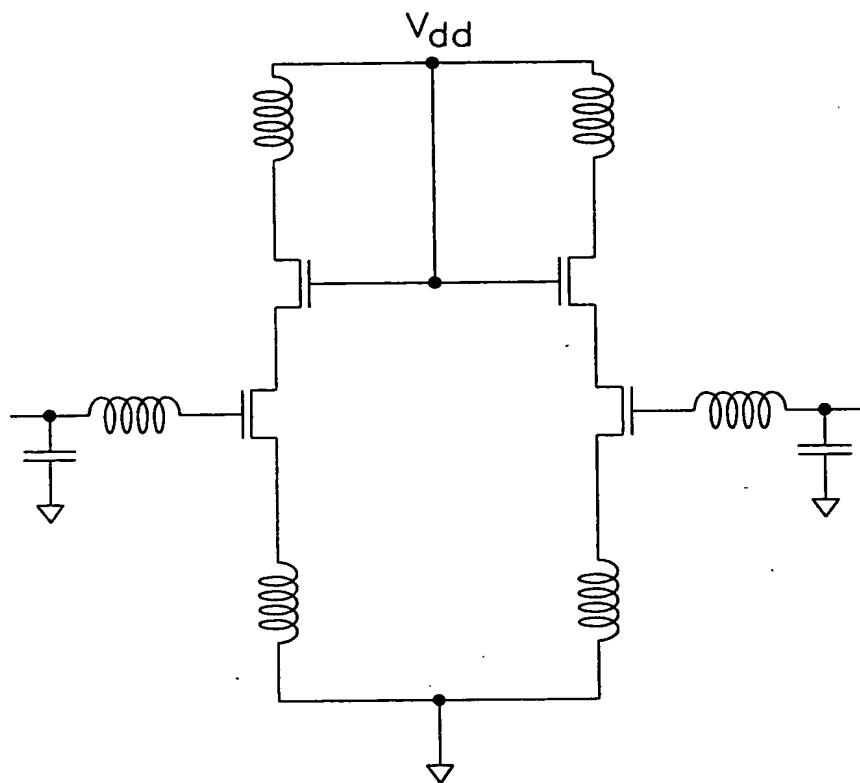
*FIG. 4(a)*

FIG. 5

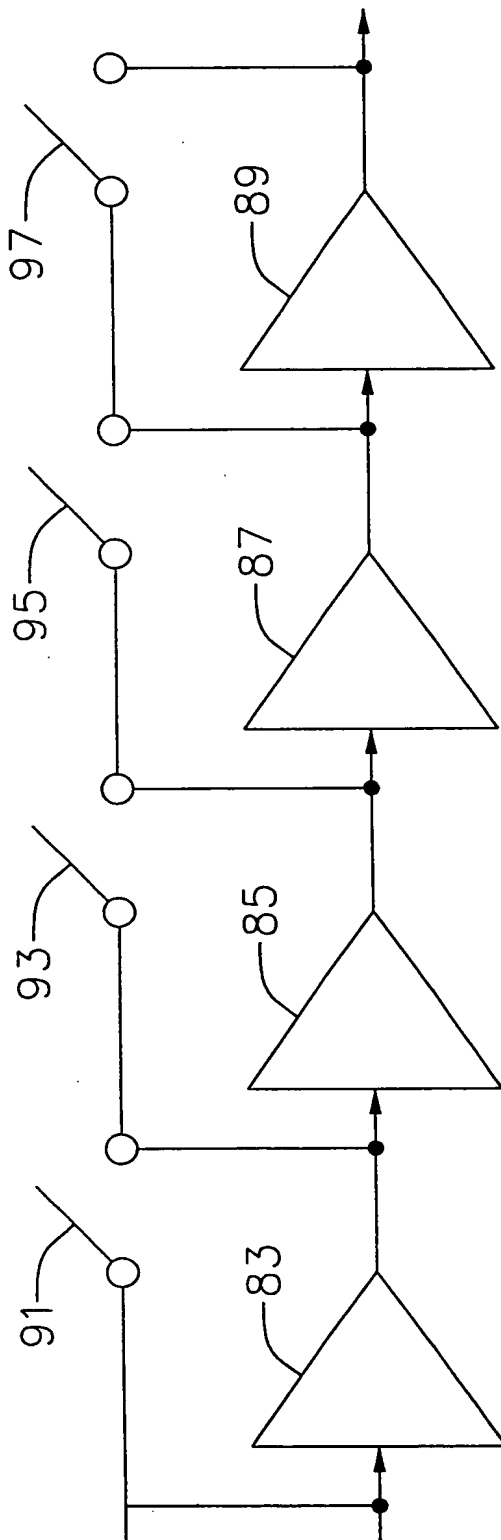
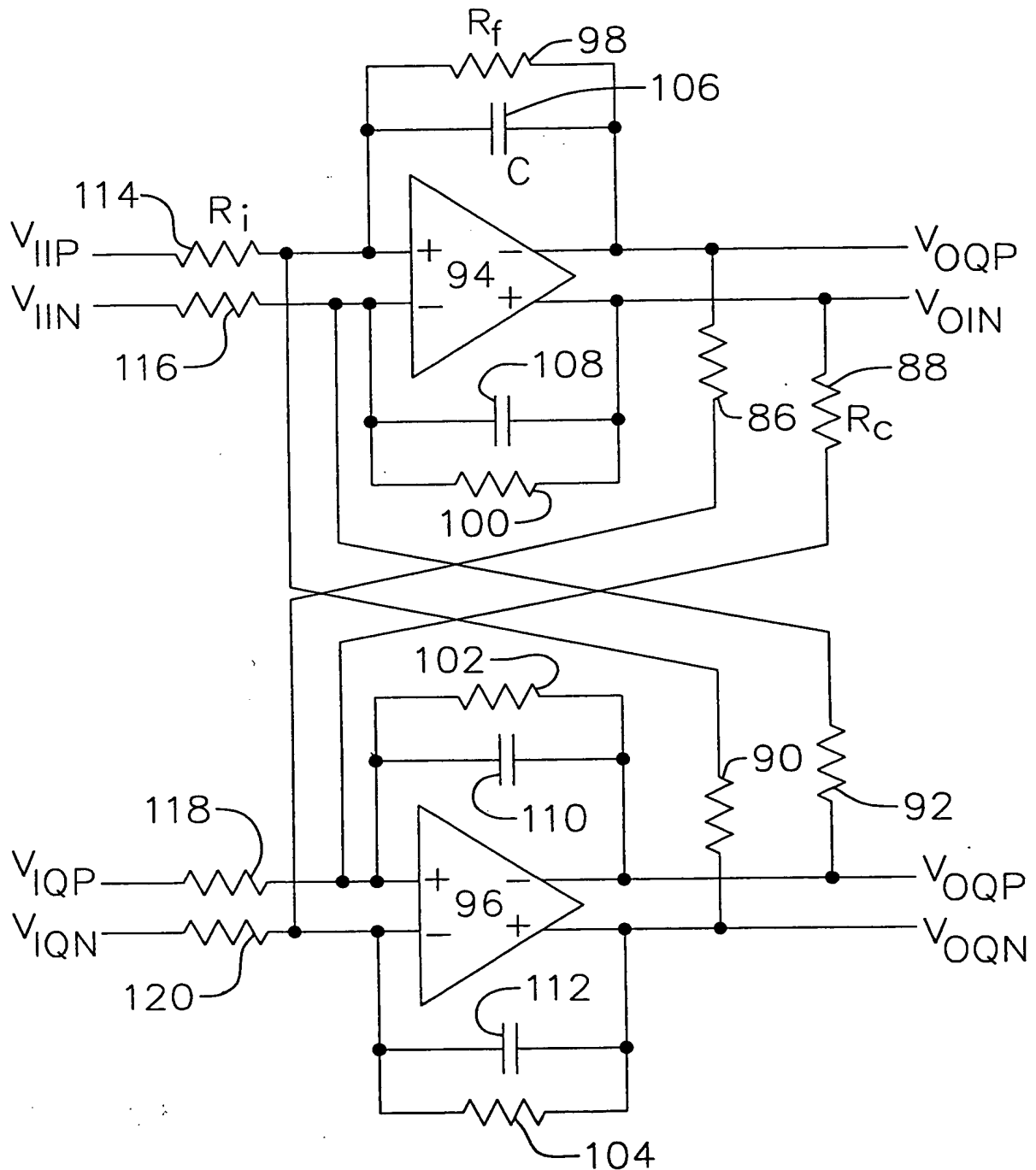
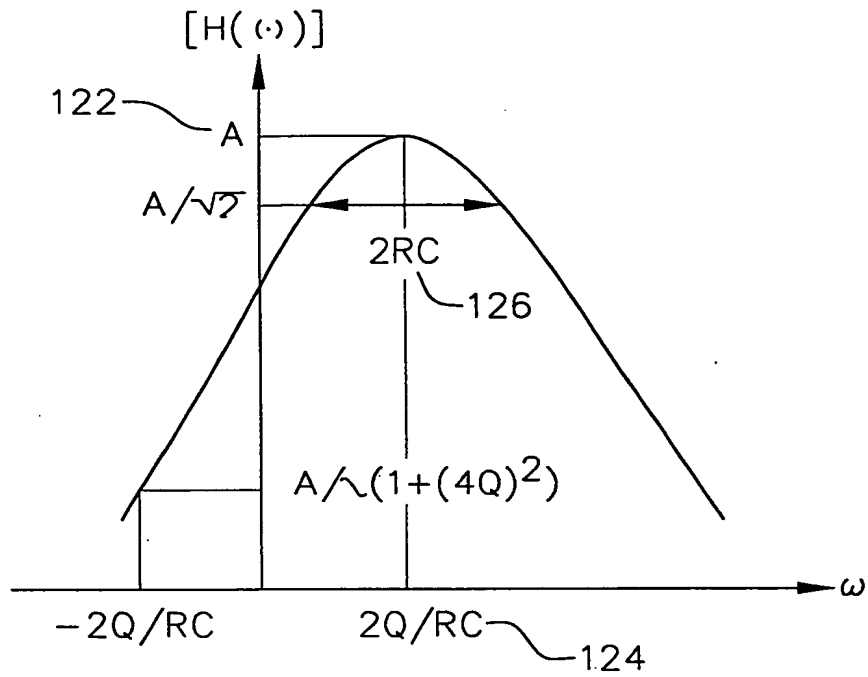


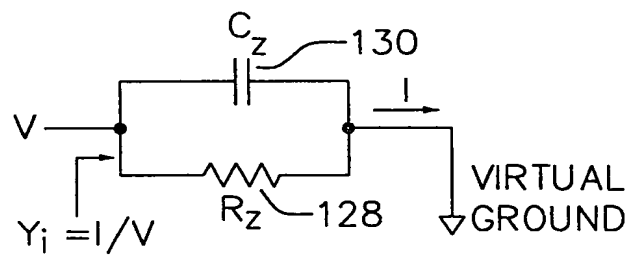
FIG. 6



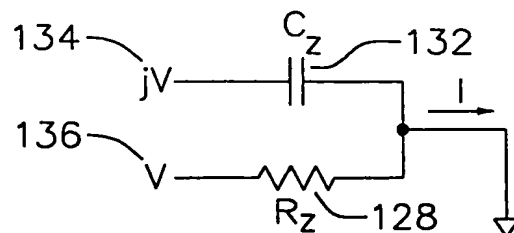
**FIG. 7**



**FIG. 8**



**FIG. 9**



**FIG. 10**

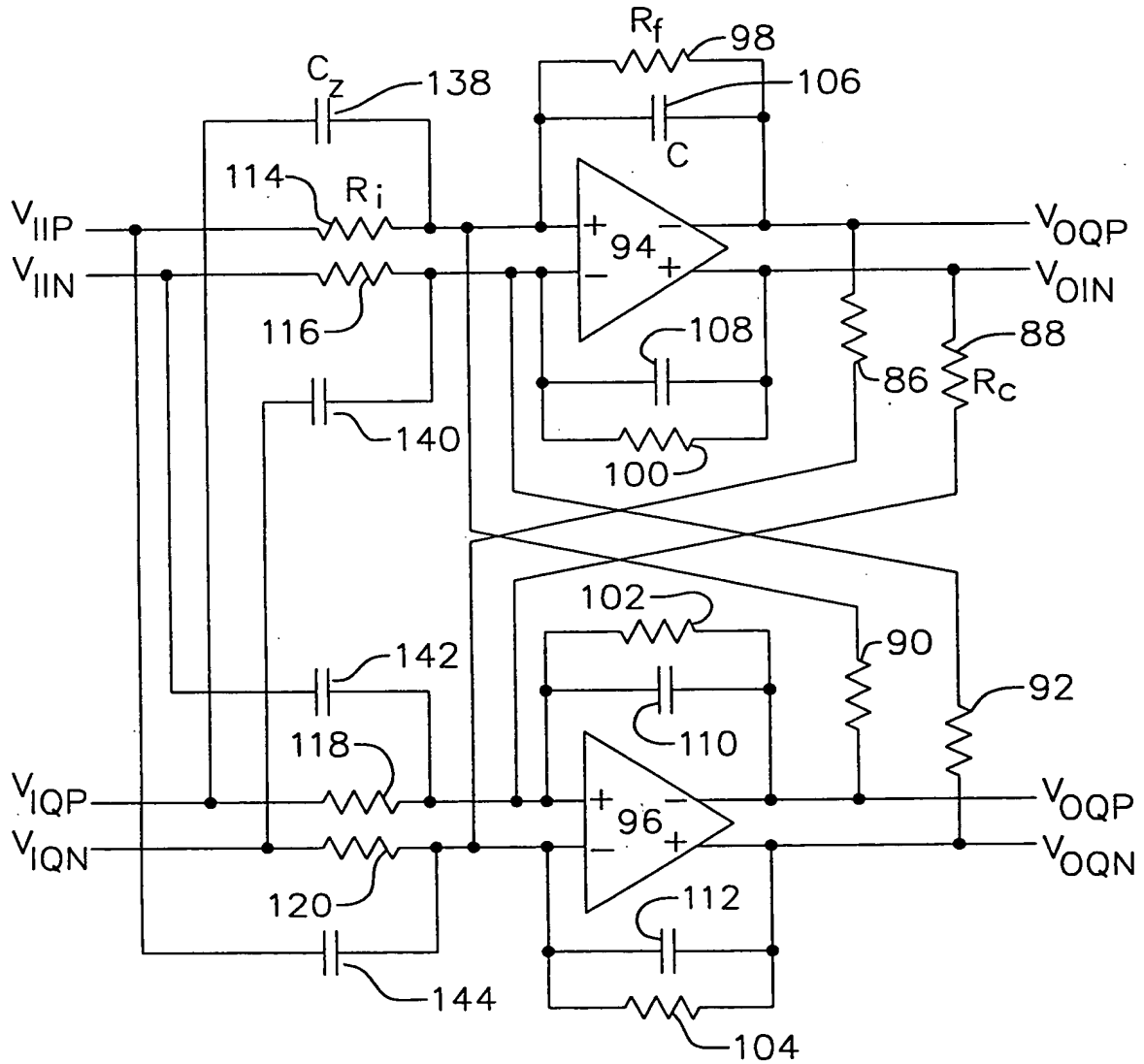
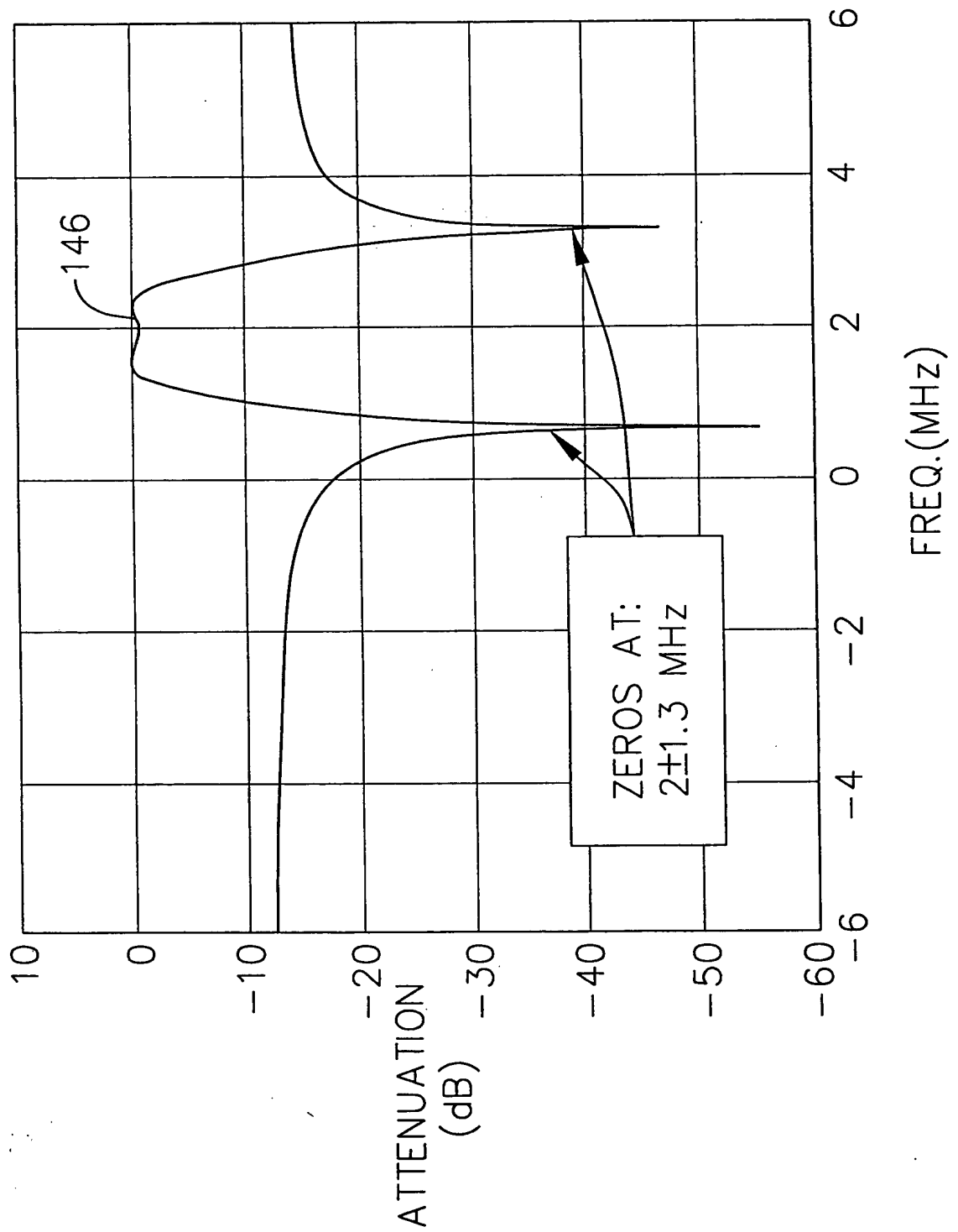




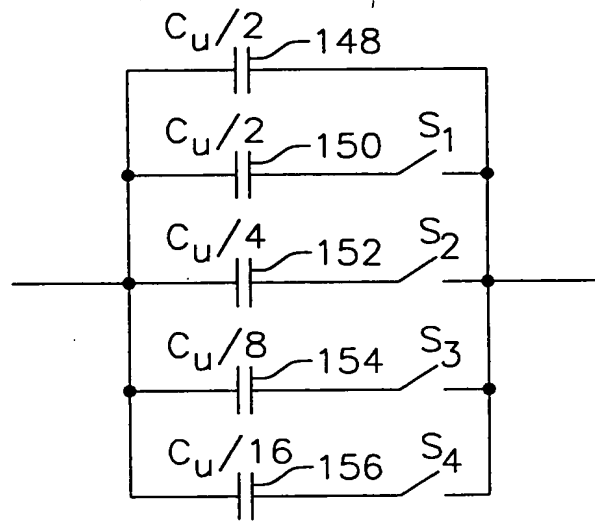
FIG. 11





10/53

*FIG. 12a*



*FIG. 12b*

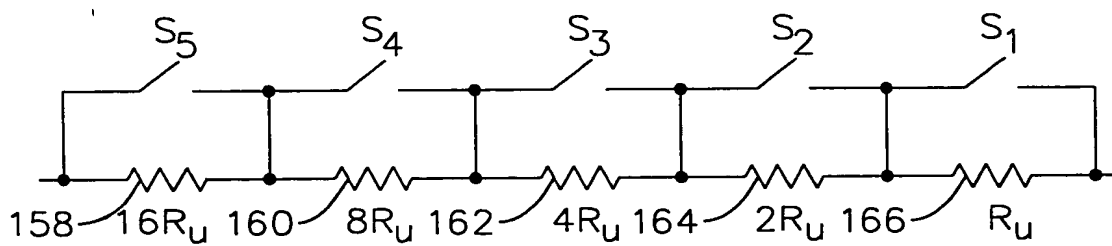


FIG. 13

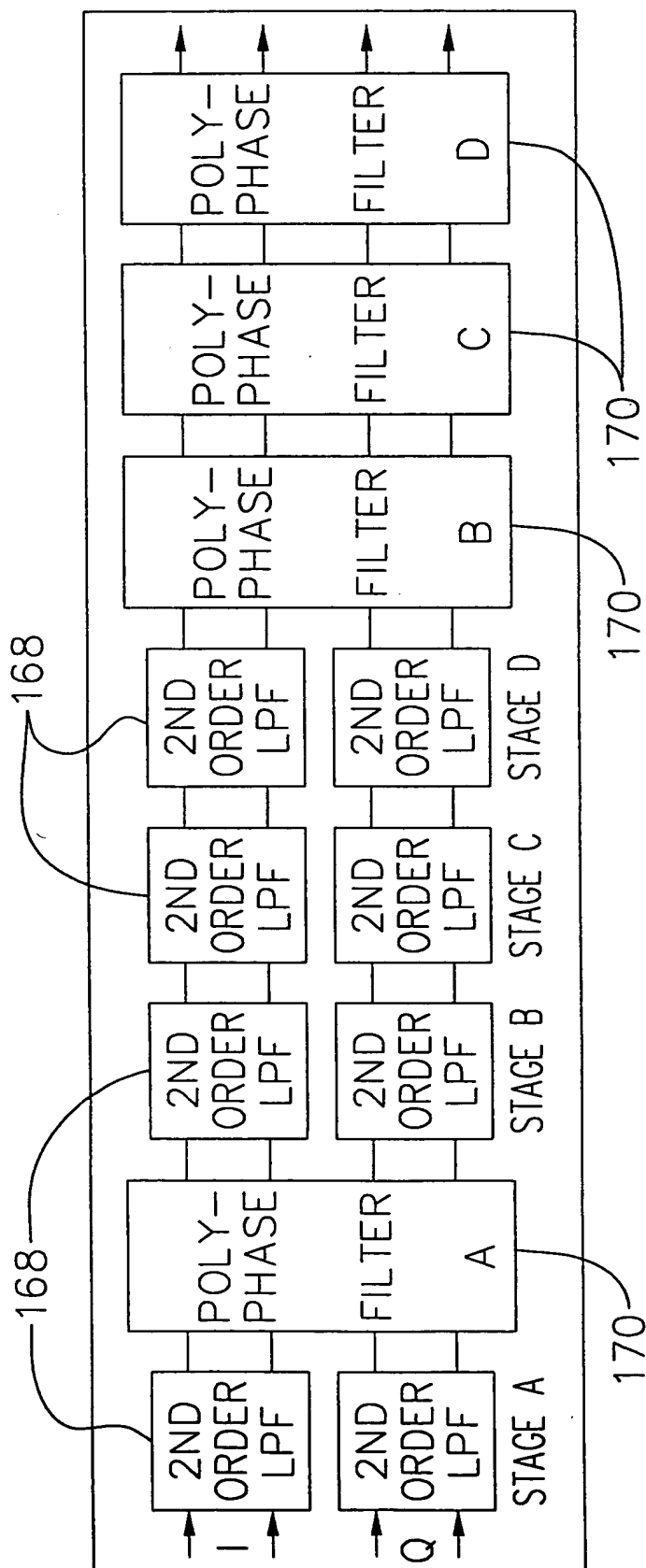
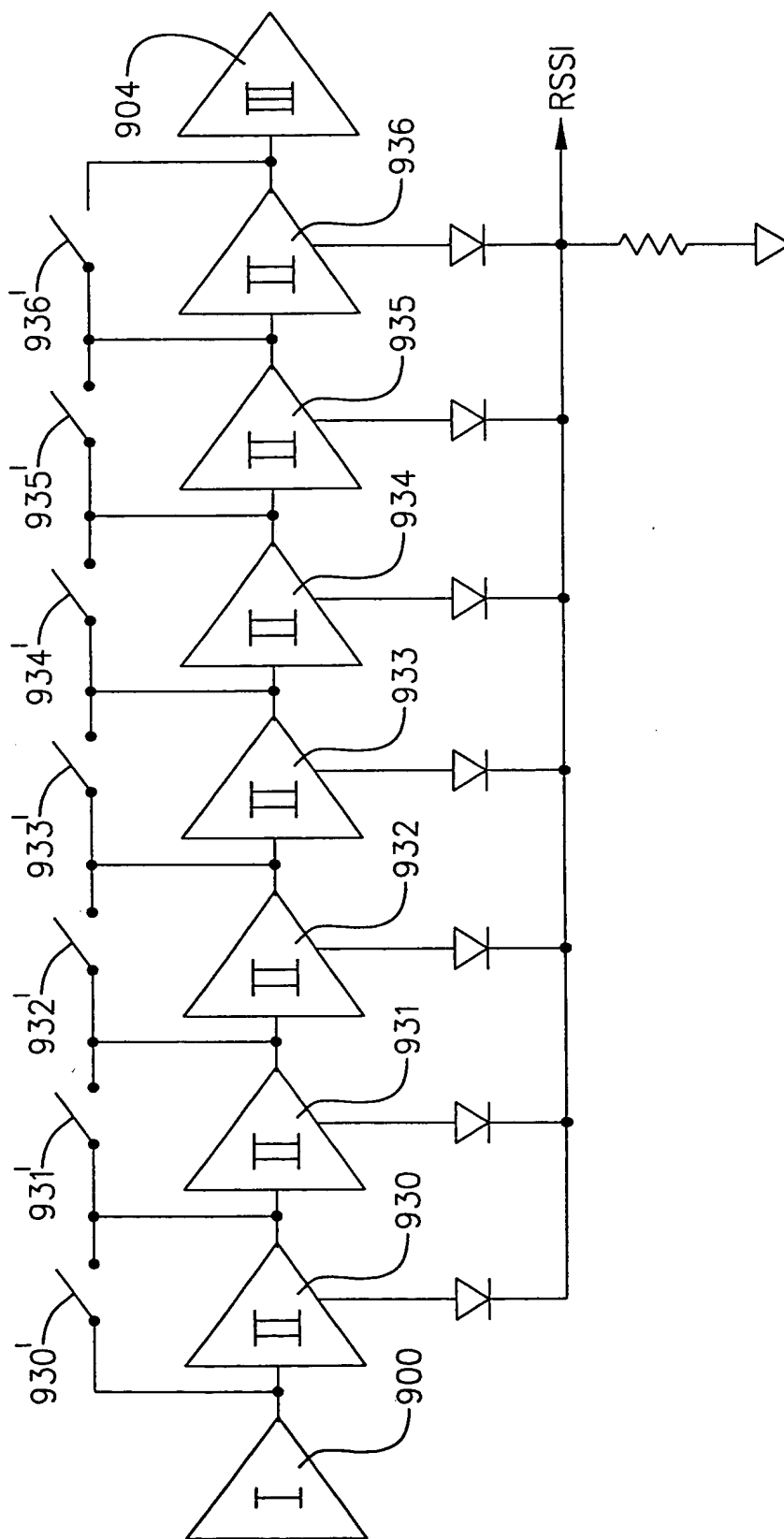
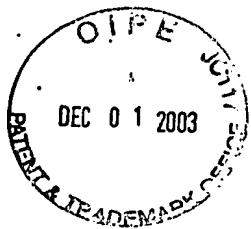
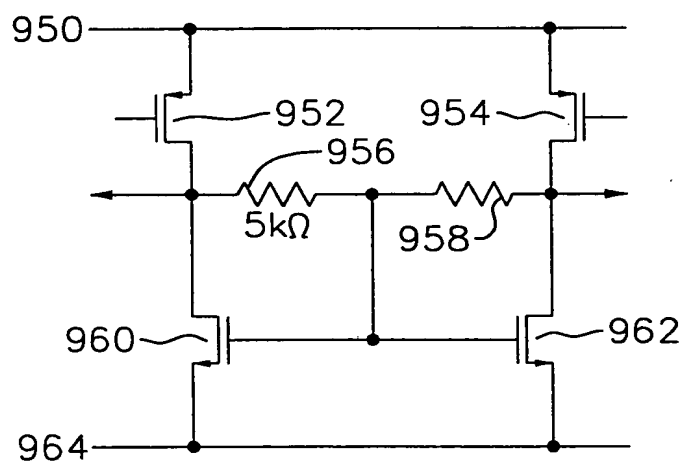
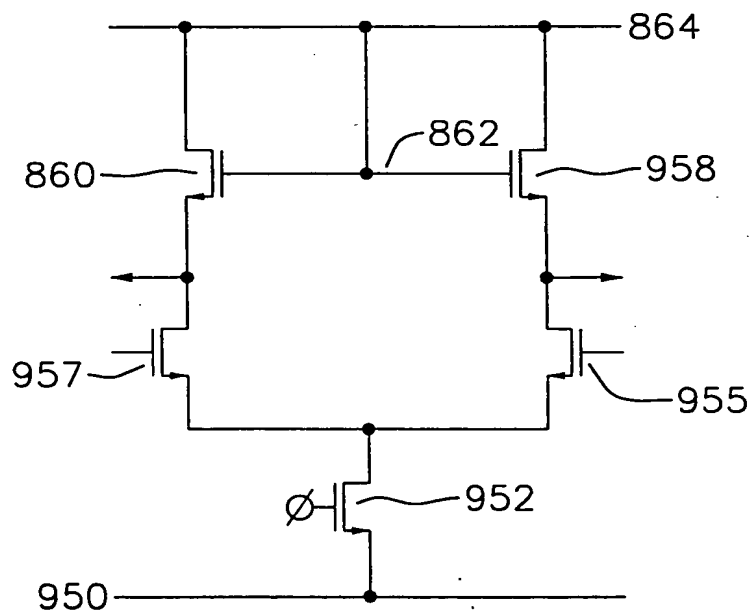
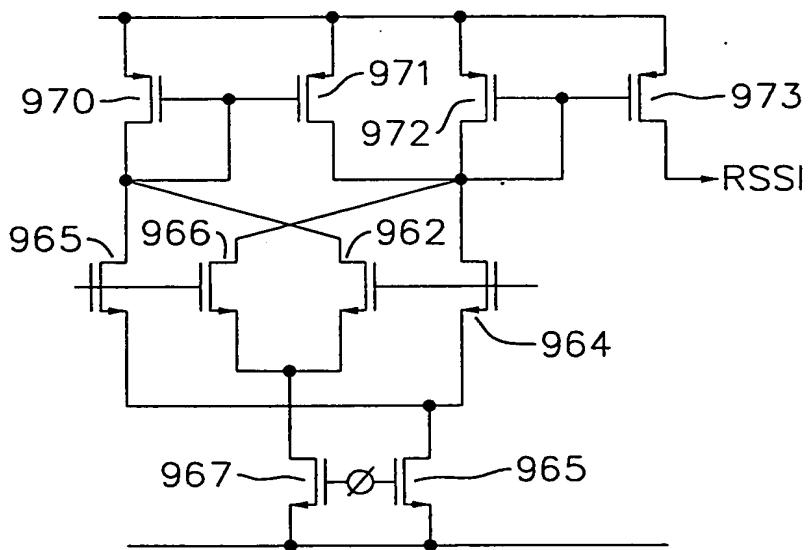


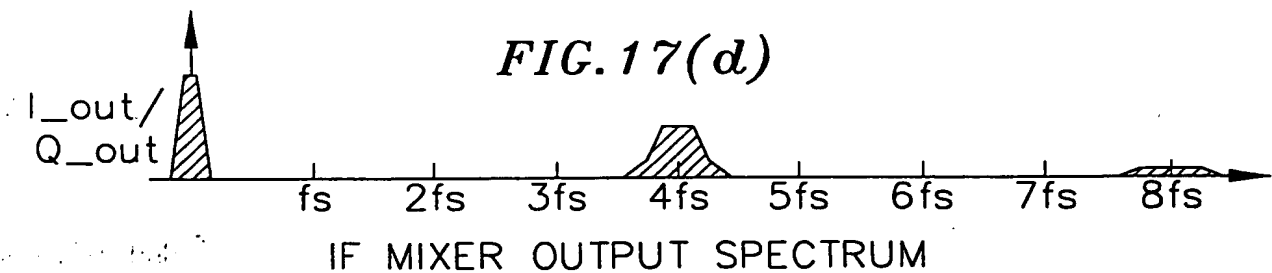
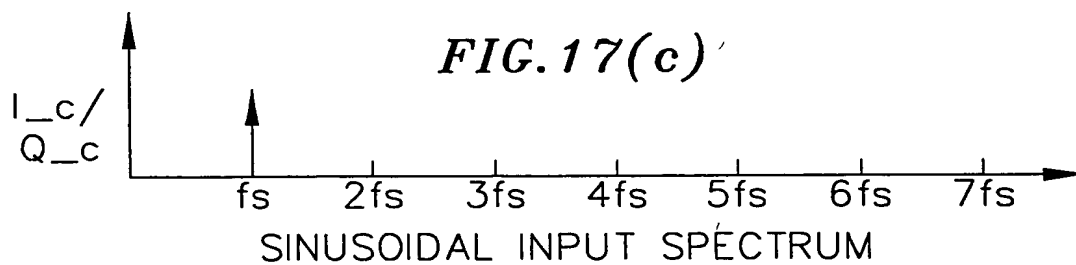
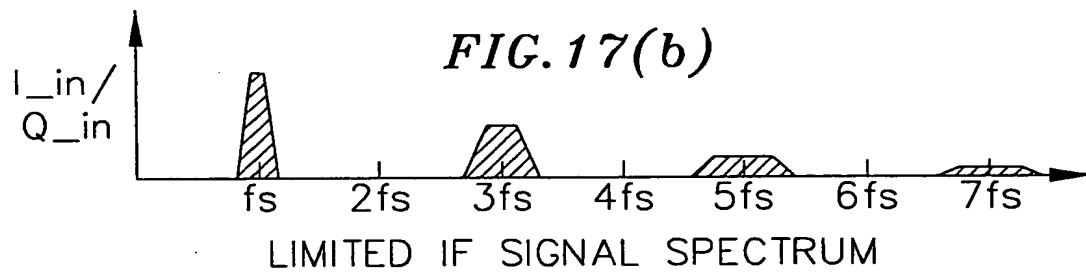
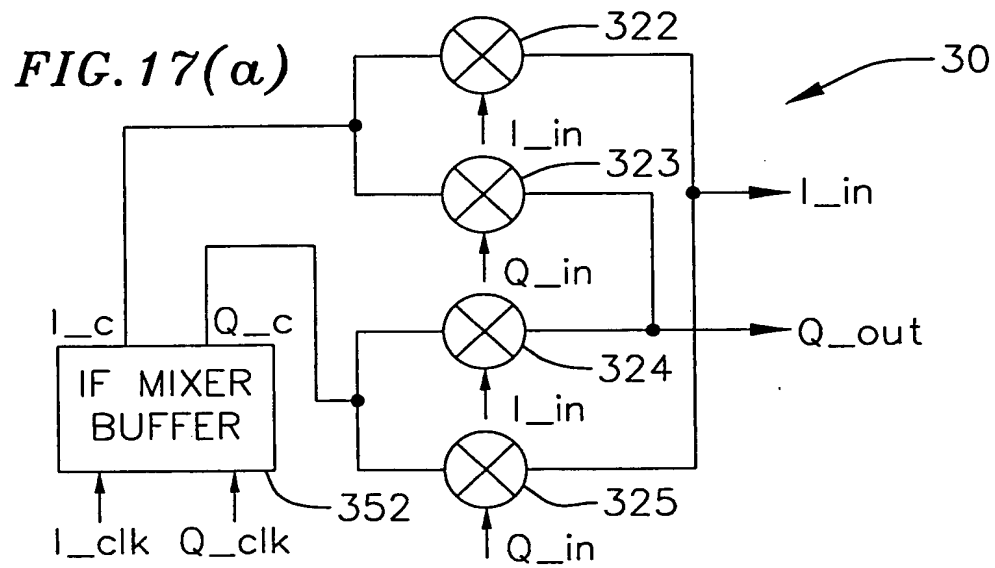
FIG. 14



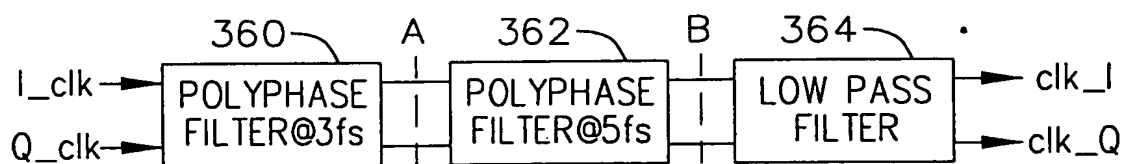
*FIG. 15**FIG. 16a*

*FIG. 16b*

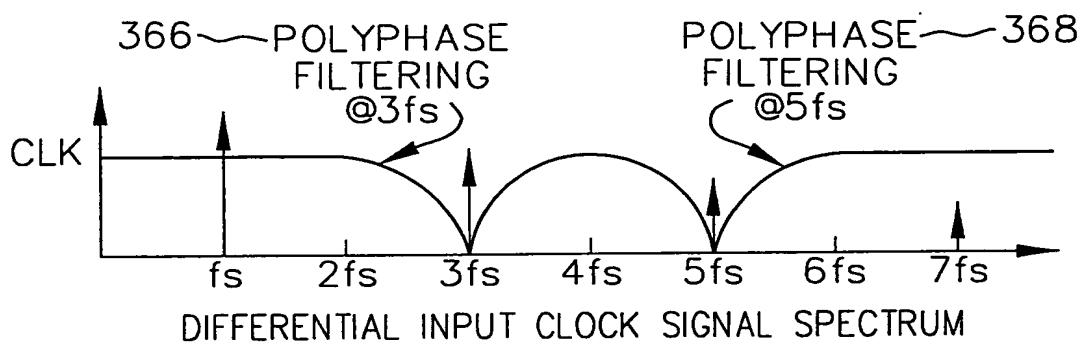




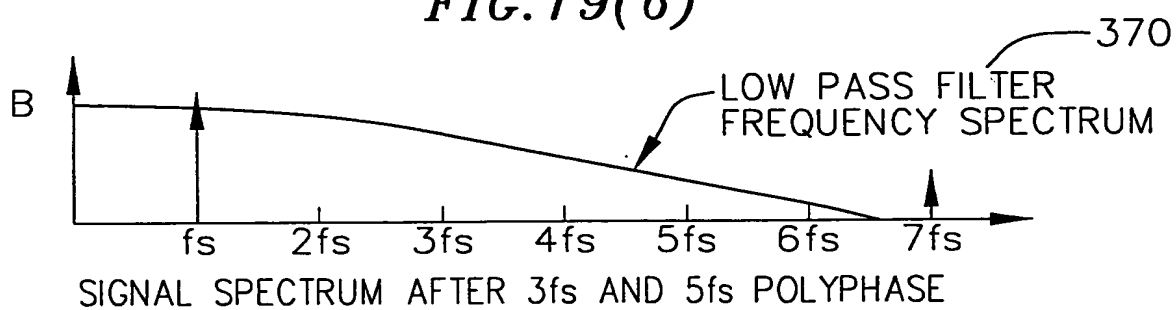
**FIG. 18**



**FIG. 19(a)**



**FIG. 19(b)**



**FIG. 19(c)**

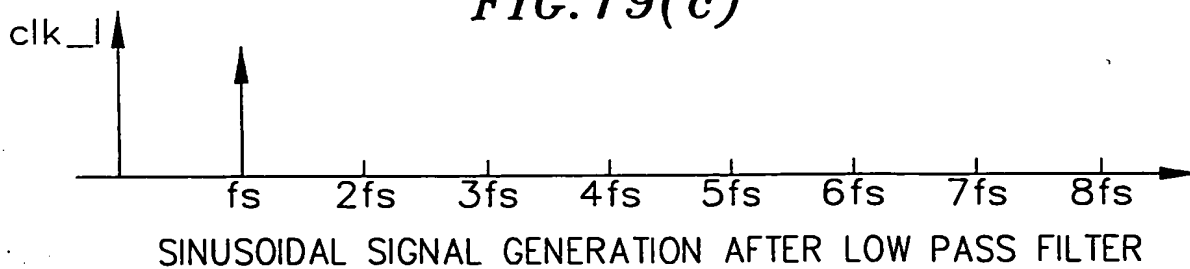
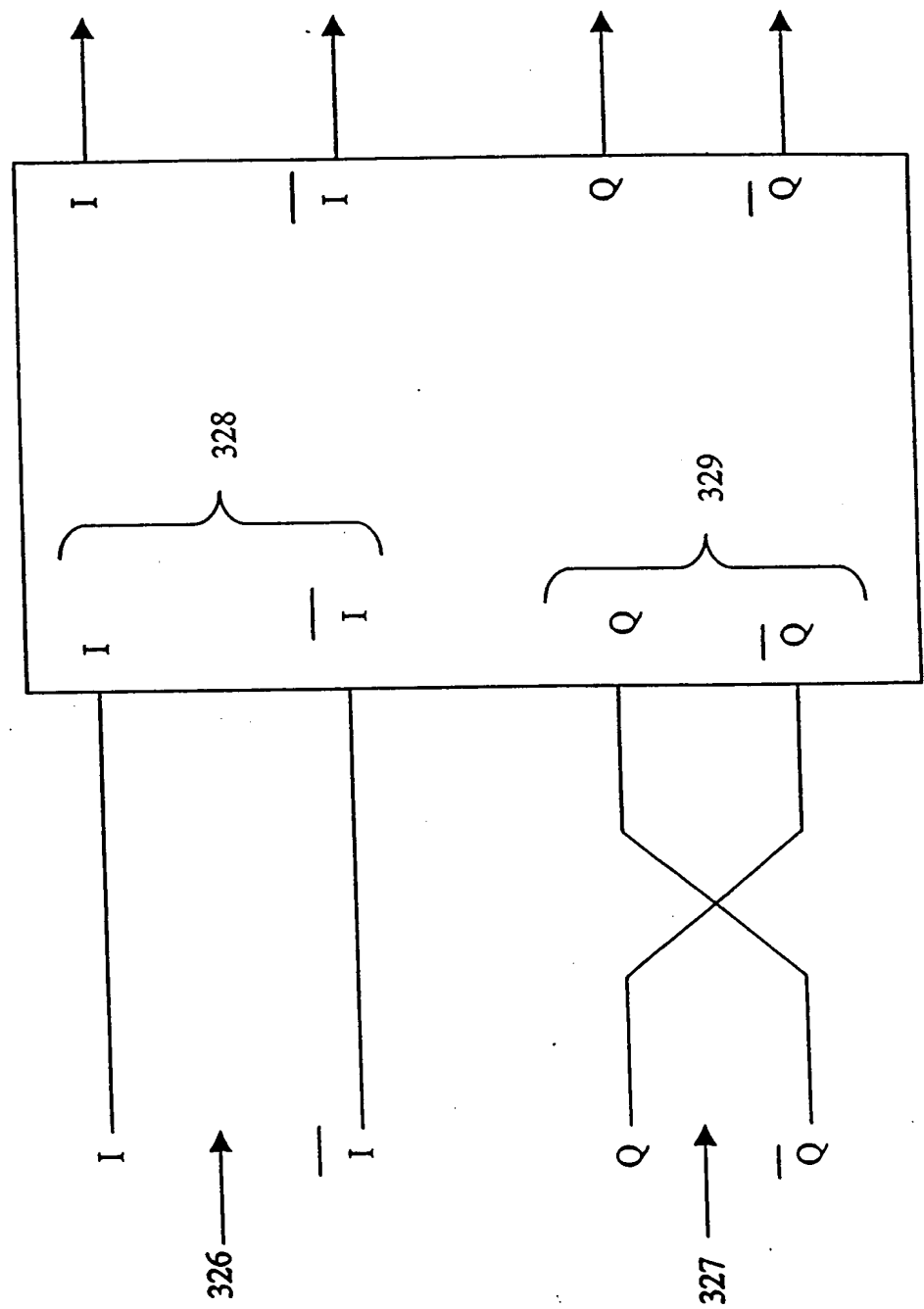
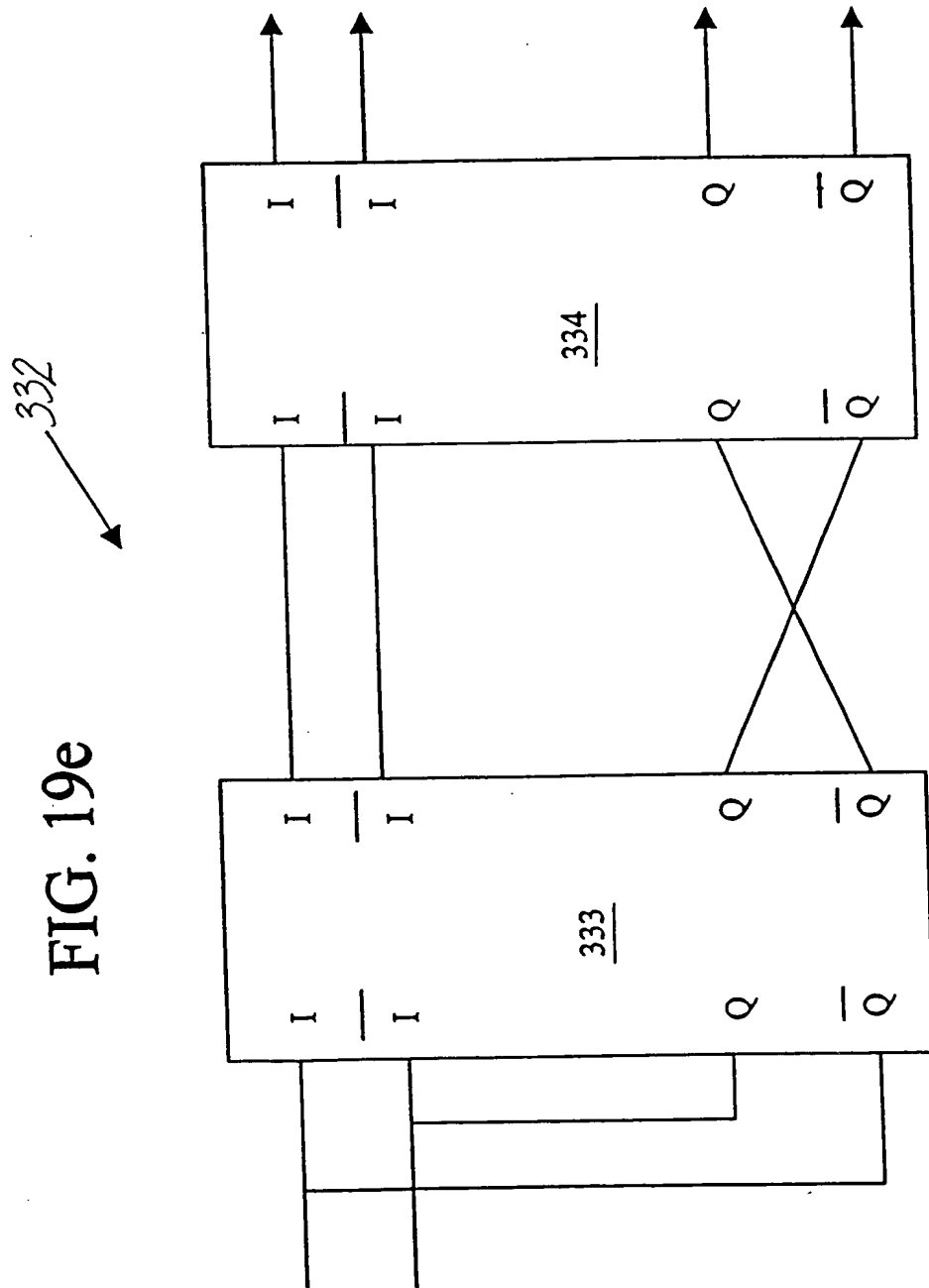


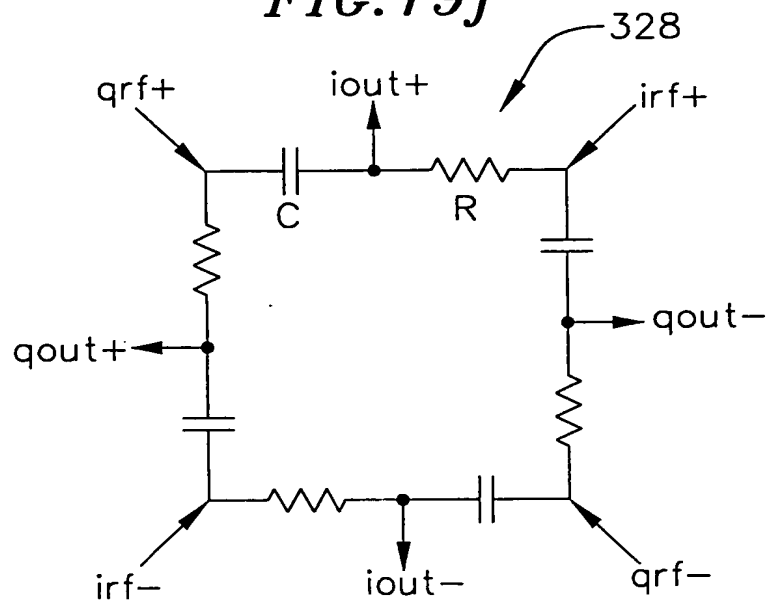


FIG. 19d

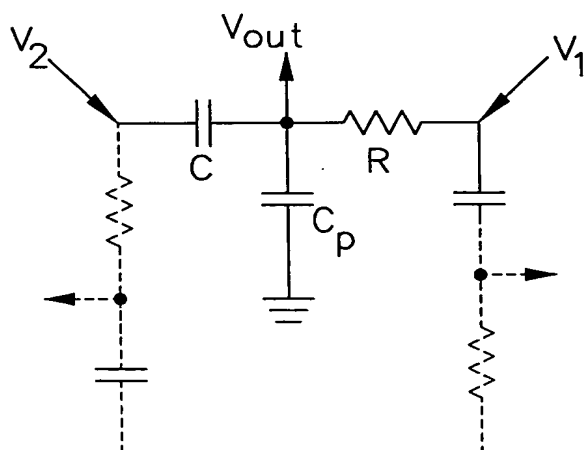




**FIG. 19f**



**FIG. 19g**

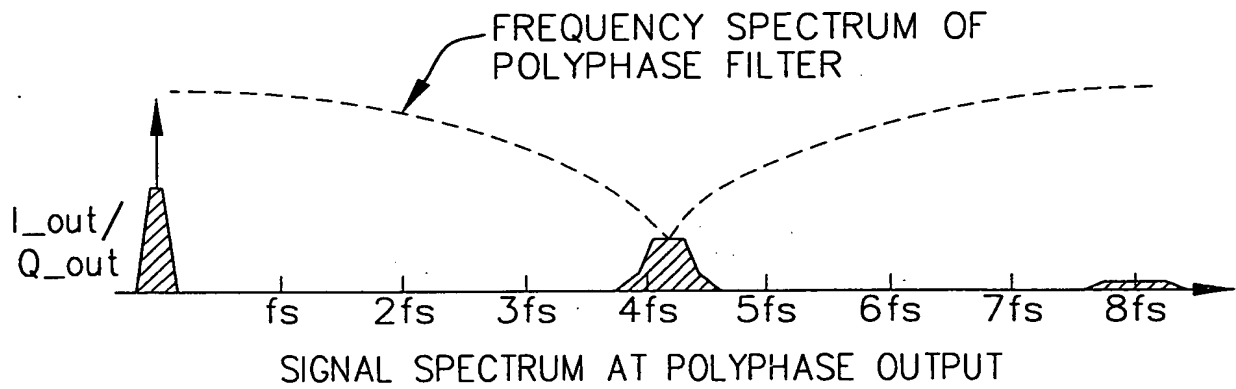


$$\omega_p = \frac{1}{R(C_p + C)}$$

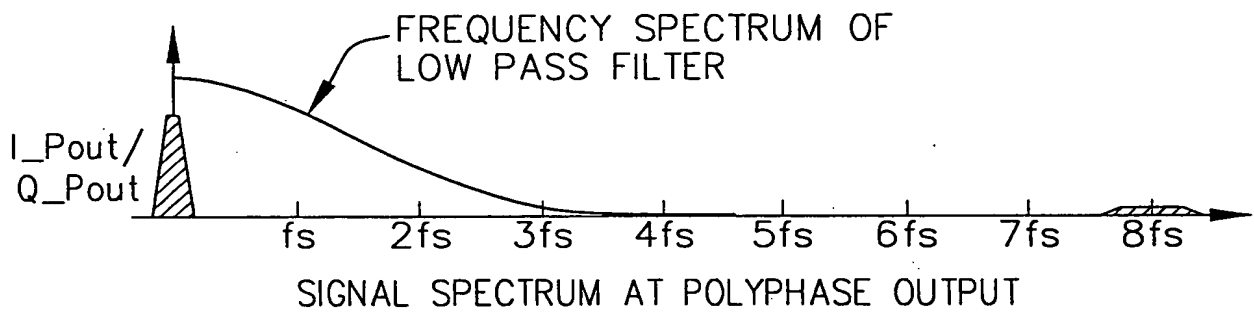
$$\omega_o = \frac{1}{RC}$$

$$V_{out} = \frac{V_1}{R(C_p + C)s + 1} + \frac{V_2 RCs}{R(C_p + C)s + 1}$$

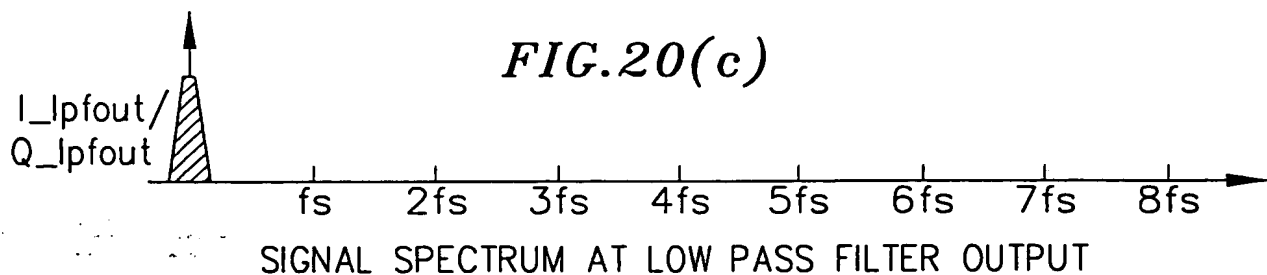
*FIG.20(a)*



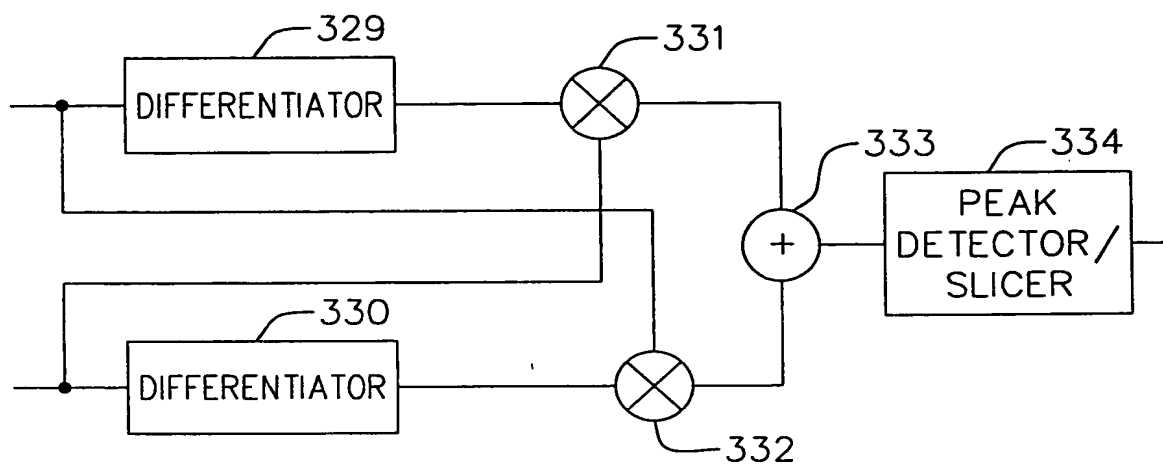
*FIG.20(b)*



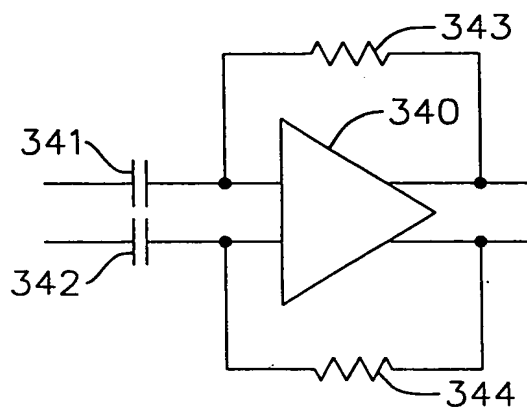
*FIG.20(c)*



*FIG. 21*



*FIG. 22*



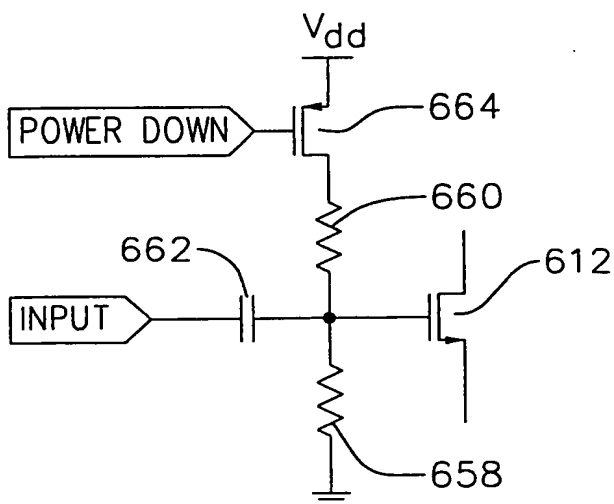
The diagram shows a crossbar switch 335. It consists of two buffers, BUFFER 1 (334) and BUFFER 2 (335). BUFFER 1 has inputs C and  $\overline{C}$ . BUFFER 2 has inputs D and  $\overline{D}$ . The circuit also includes two PMOS transistors (340, 342) connected to VDD, two NMOS transistors (344, 346) connected to ground, and two NMOS transistors (348, 350) connected to ground. The output is taken from the node between the PMOS and NMOS transistors.

[illegible]

The diagram shows an on-chip differential amplifier circuit. The input stage consists of a differential pair of NMOS transistors (612, 614) with a common source resistor (616) connected to a Bias source. The gates of the input transistors are driven by a differential-mode input signal (Inp) and a common-mode input signal (Inn). The output of the input stage is taken differentially from the drains of transistors 612 and 614. The output signals are coupled through capacitors (628, 624) and inductors (624, 622) to a second differential pair of NMOS transistors (632, 634). The gates of the second pair are driven by a differential-mode input signal (Inp) and a common-mode input signal (Inn). The output of the second stage is taken differentially from the drains of transistors 632 and 634. The output signals are coupled through capacitors (642, 646) and inductors (648, 644) to a balun (654) and a 50 ohm termination resistor (650). The balun is connected to a 50 ohm termination resistor (654) and a 50 ohm termination resistor (650). The output signals are taken differentially from the balun output (652) and the 50 ohm termination resistor (650).

# ON-CHIP

*FIG. 26a*



*FIG. 26b*

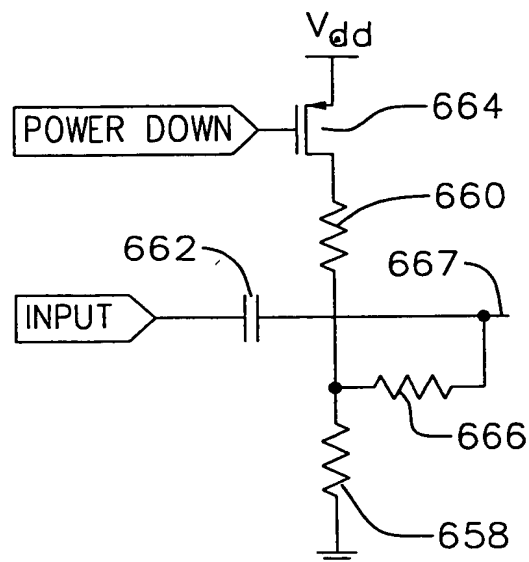
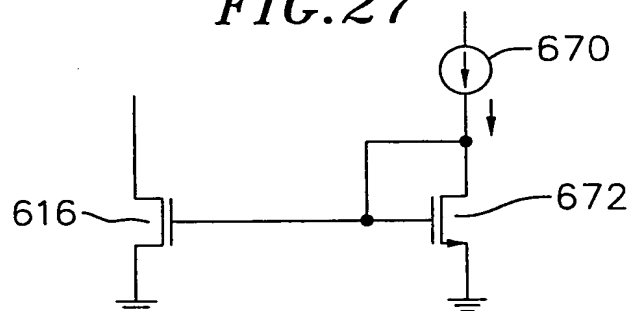


FIG. 27



**FIG. 28**

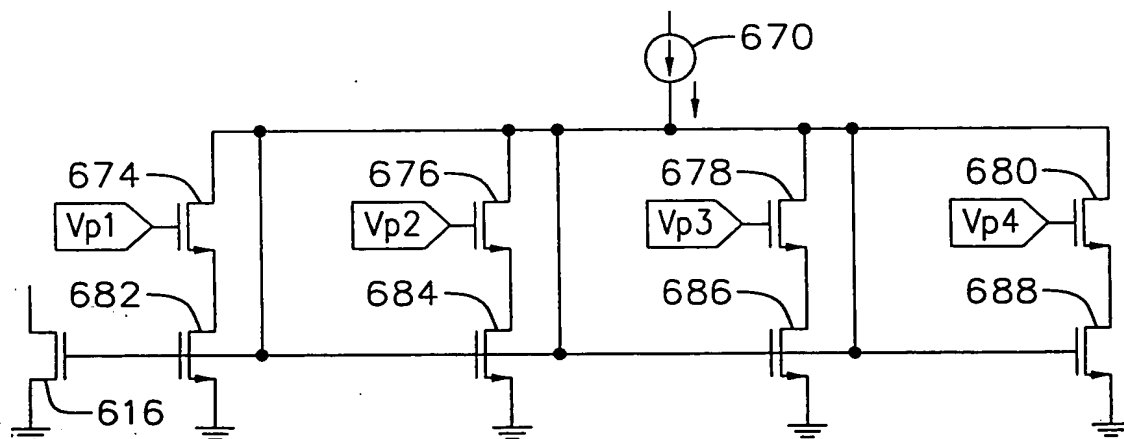




FIG. 29

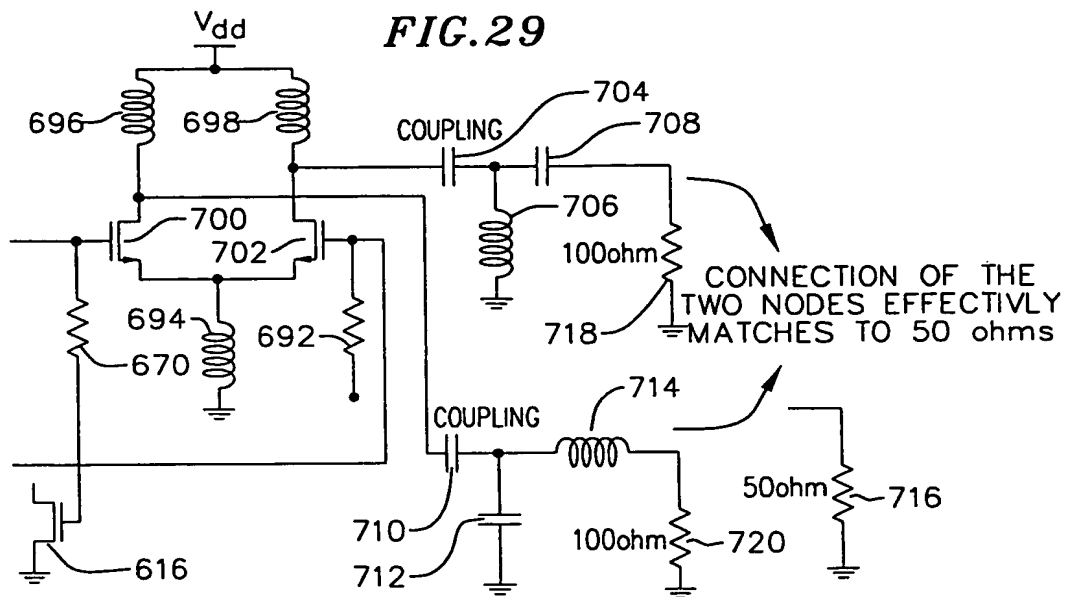
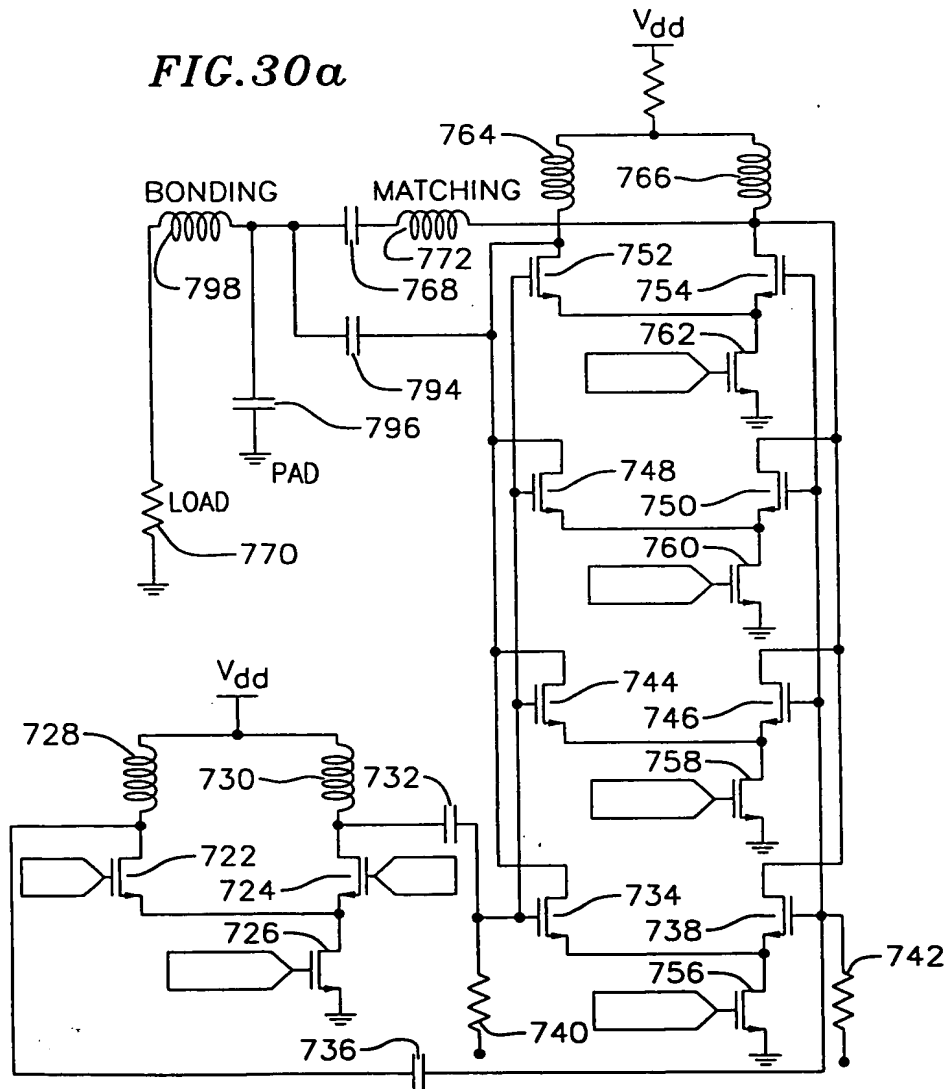


FIG. 30a



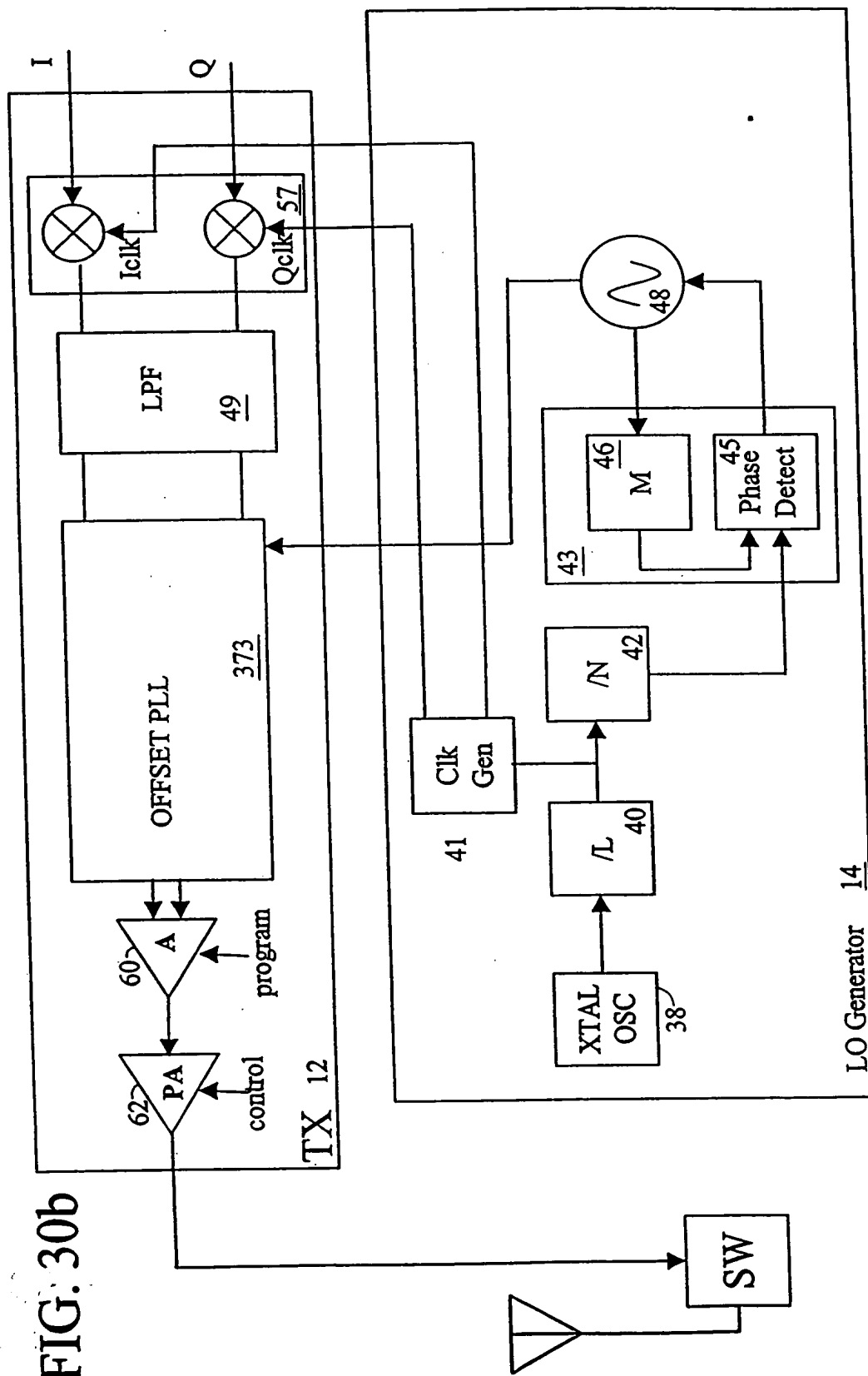


FIG. 30b

FIG. 30c

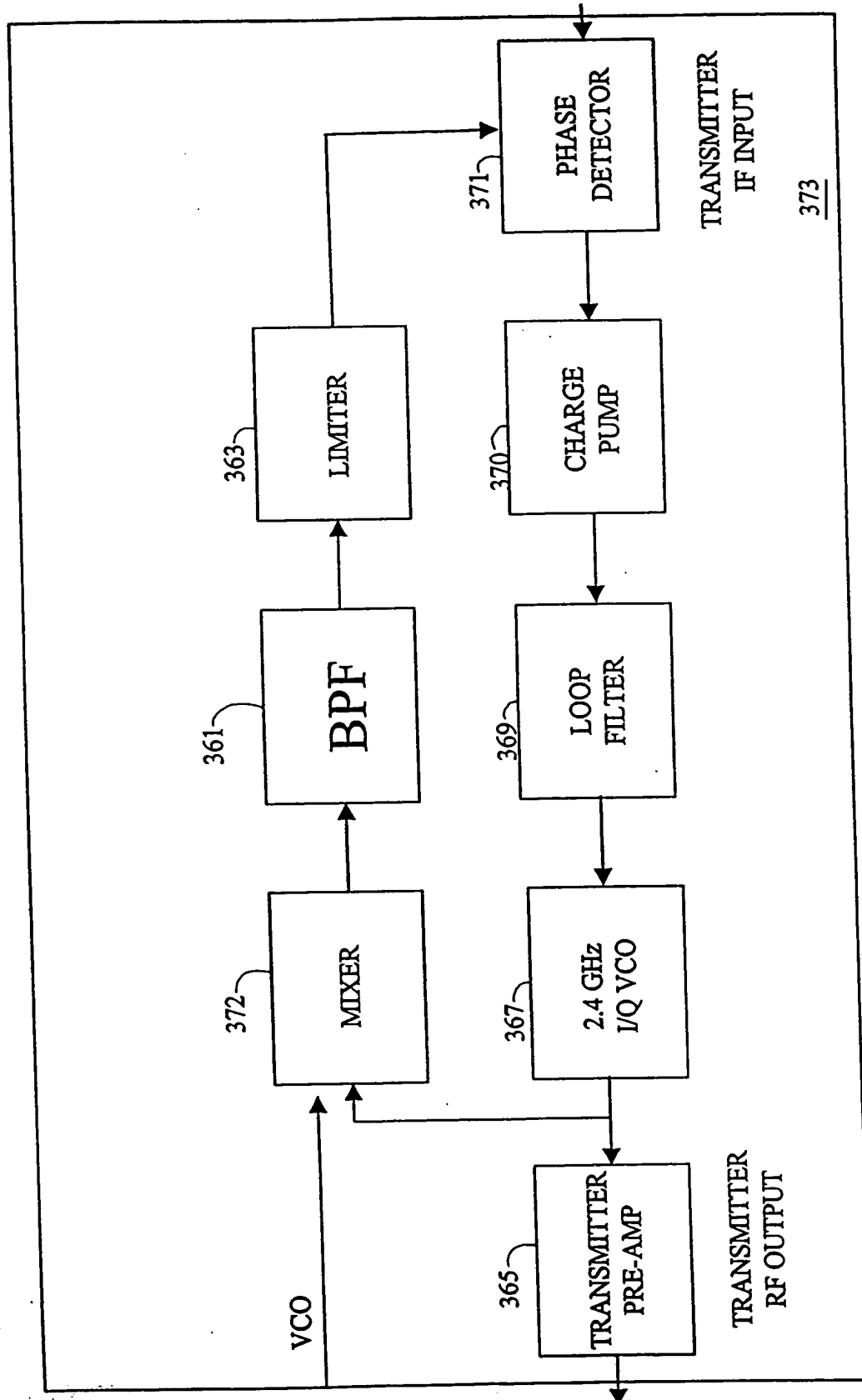
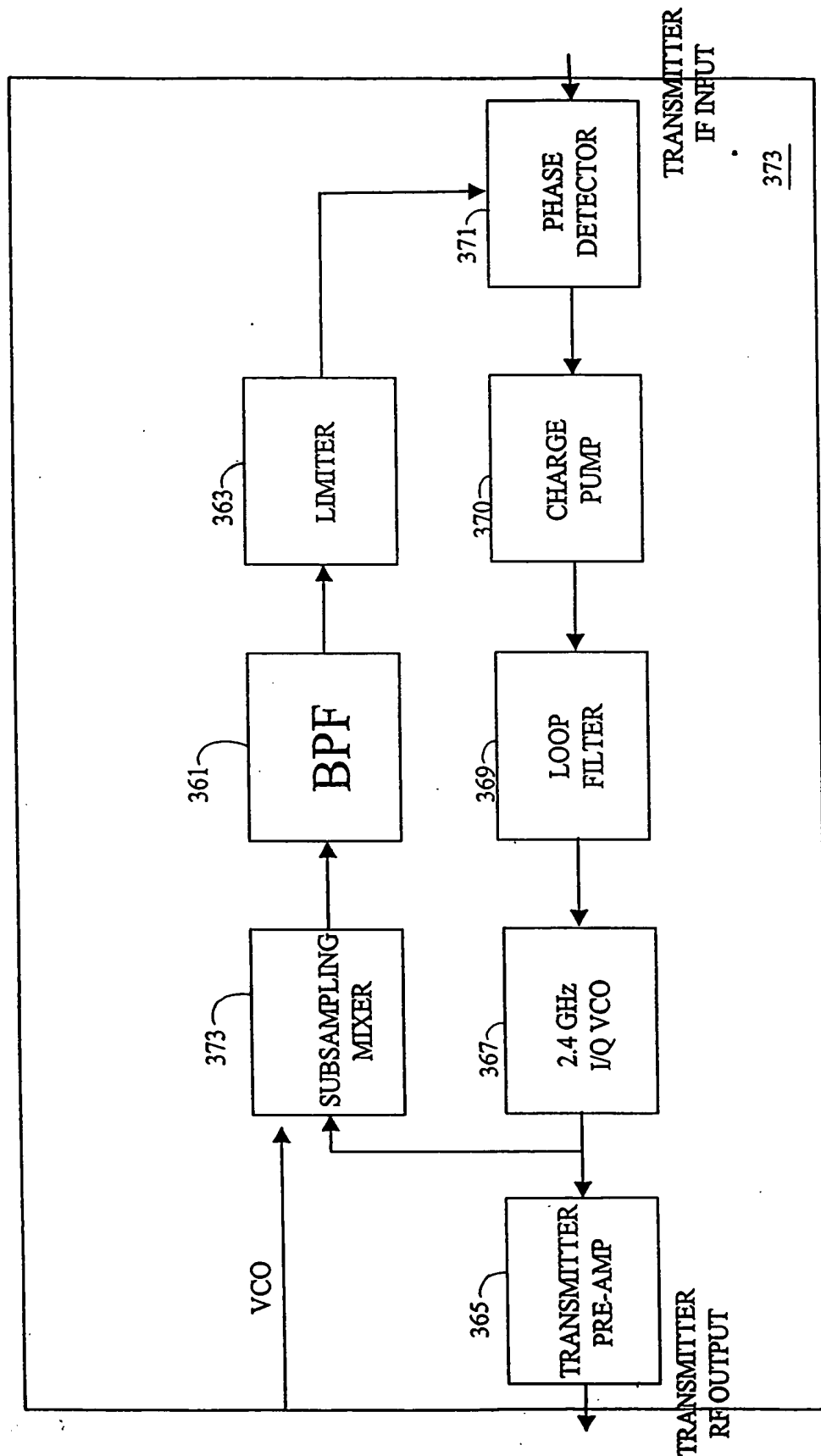
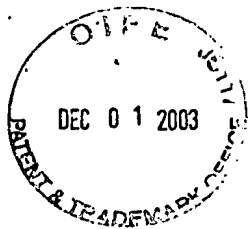
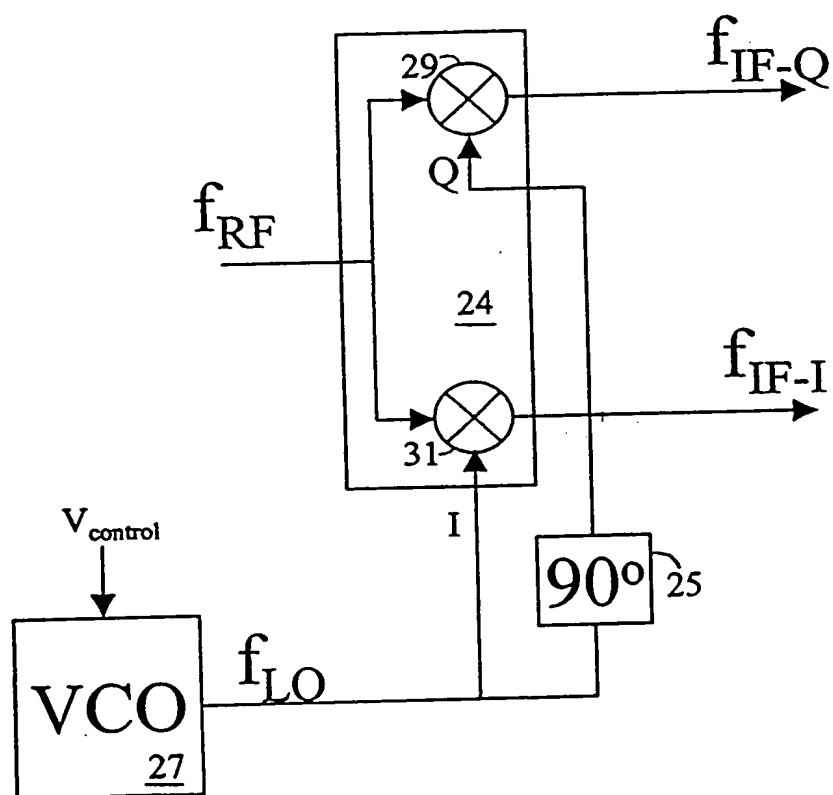
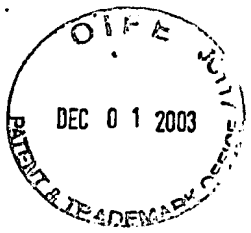
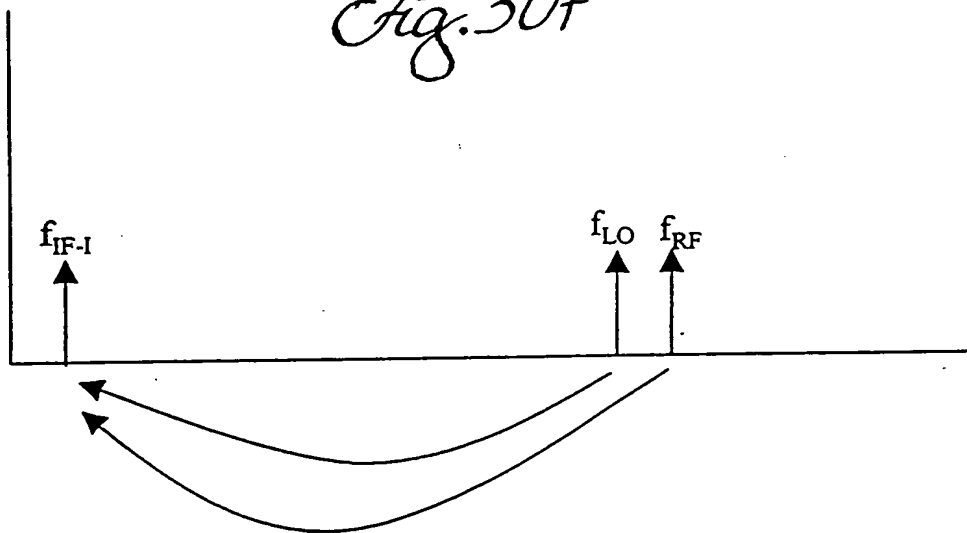
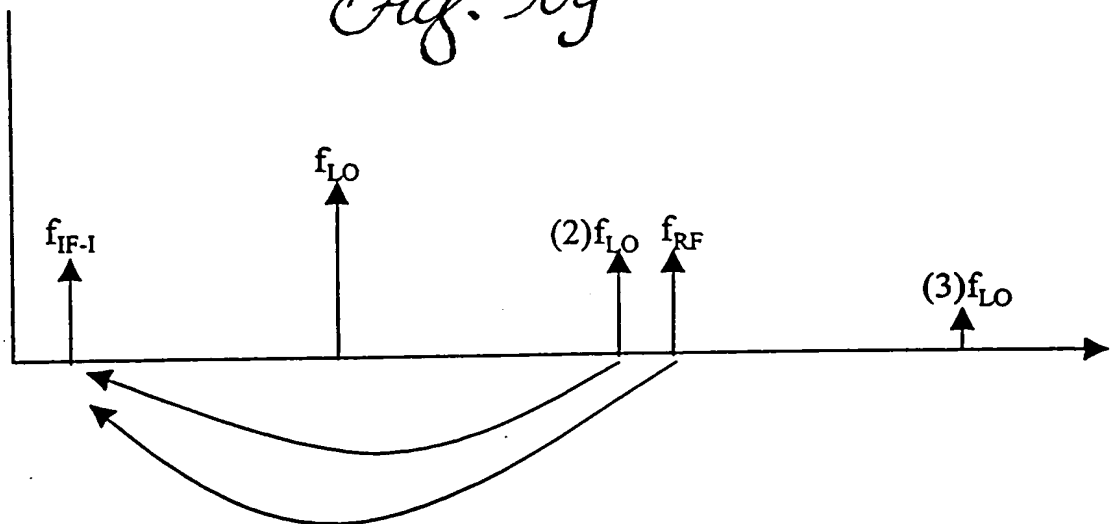
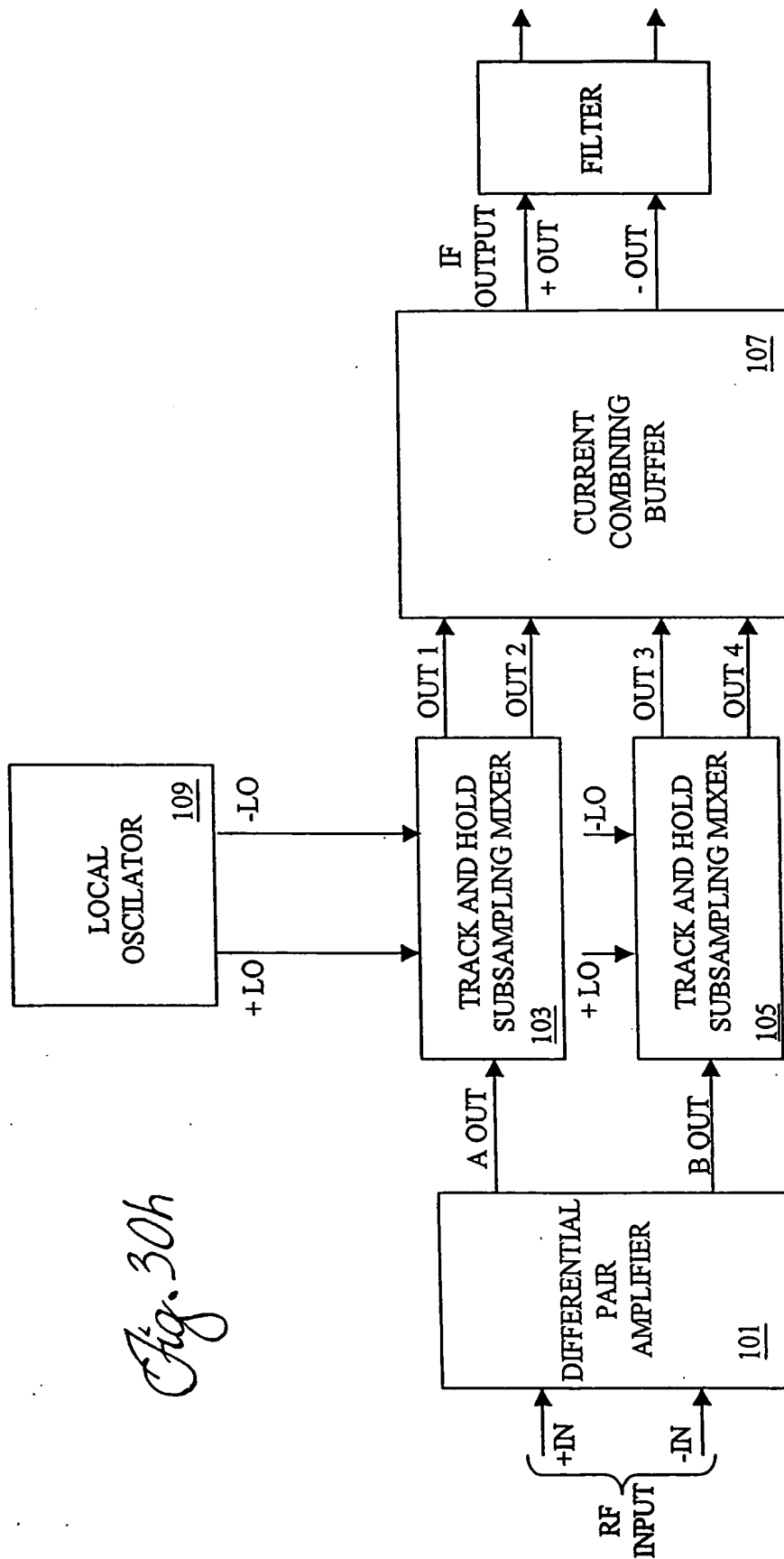


FIG. 30d



*Fig. 30e*

*Fig. 30f**Fig. 30g*



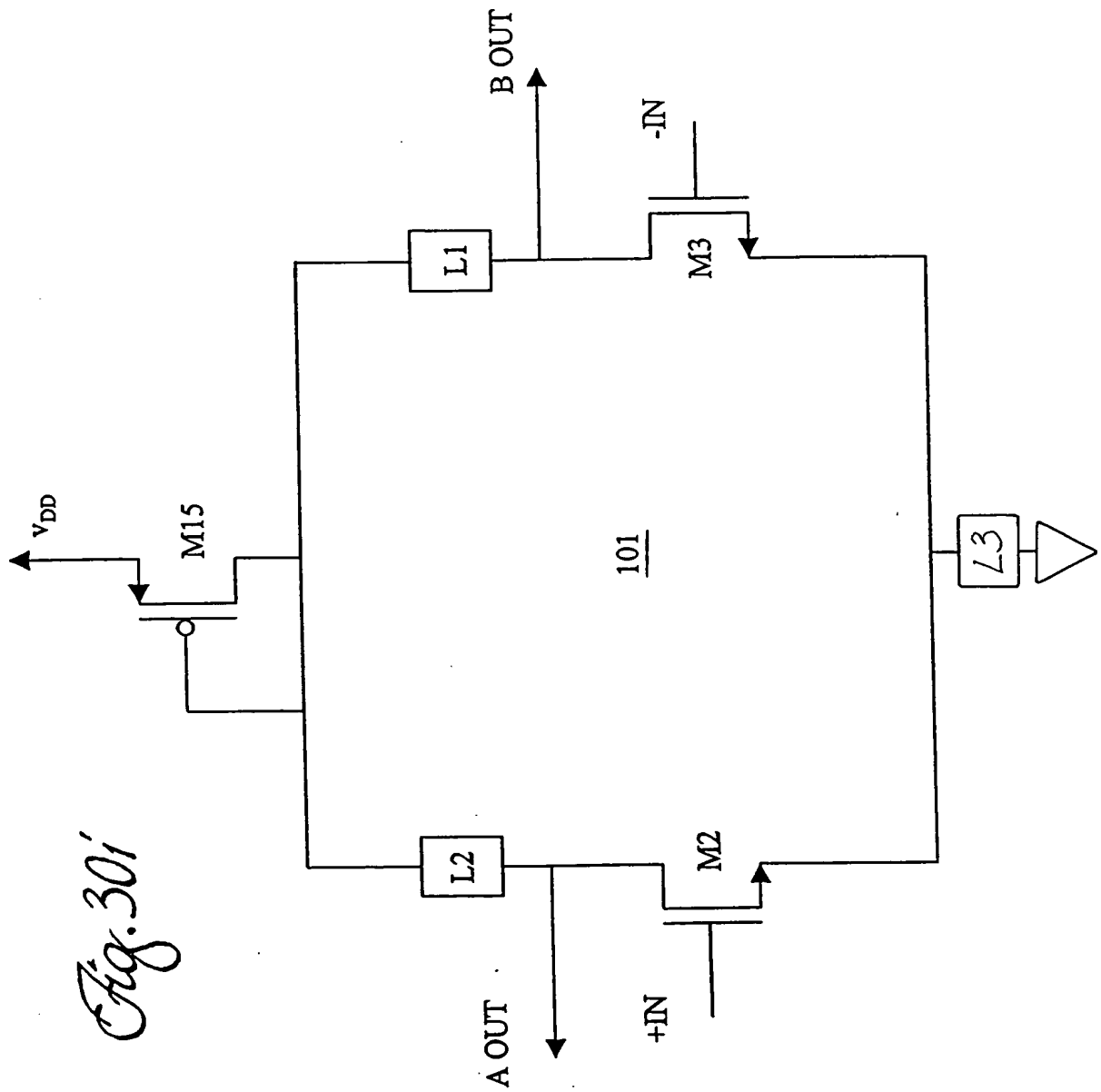






Fig. 30j

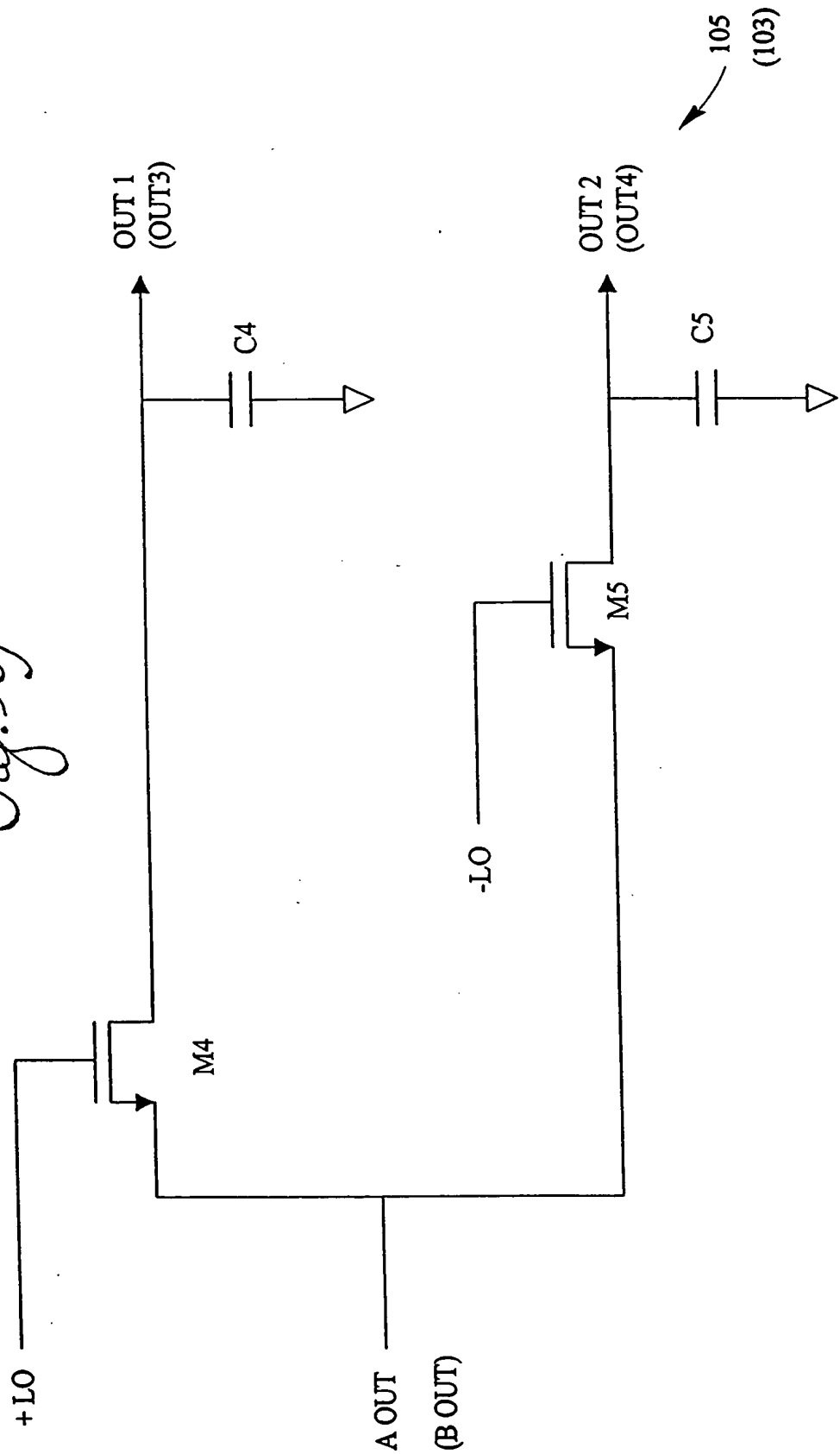


Fig. 30k

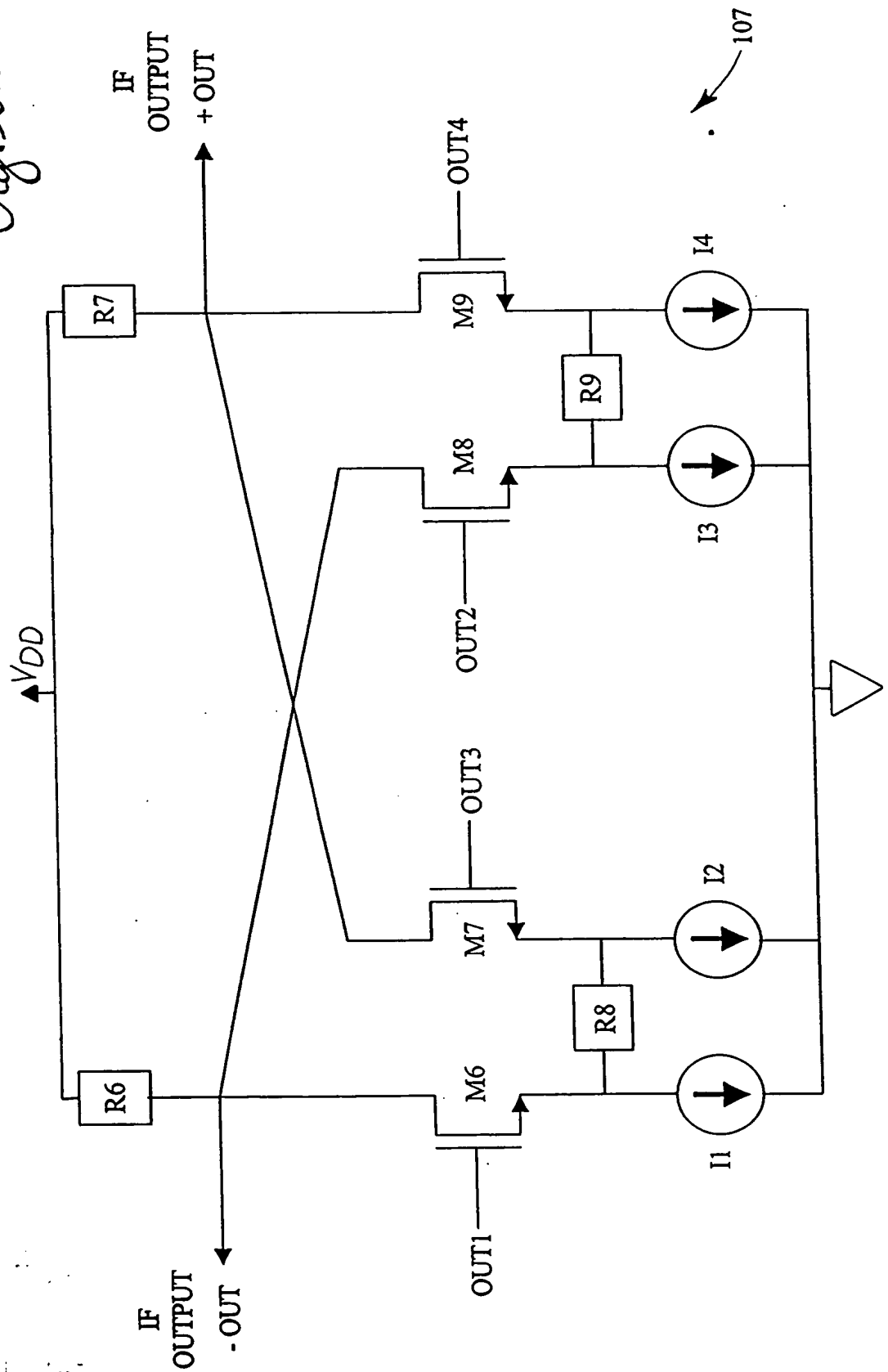
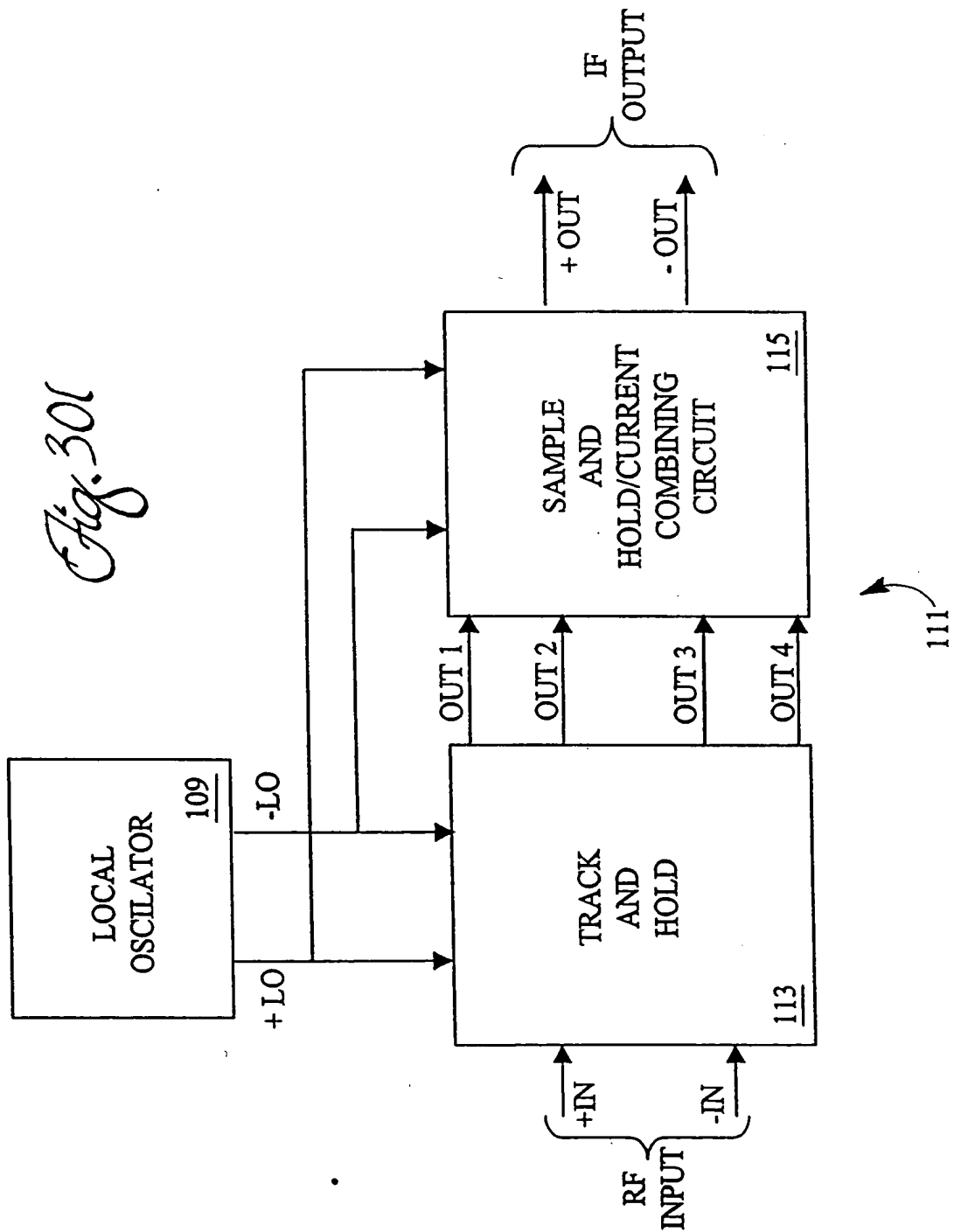


Fig. 301



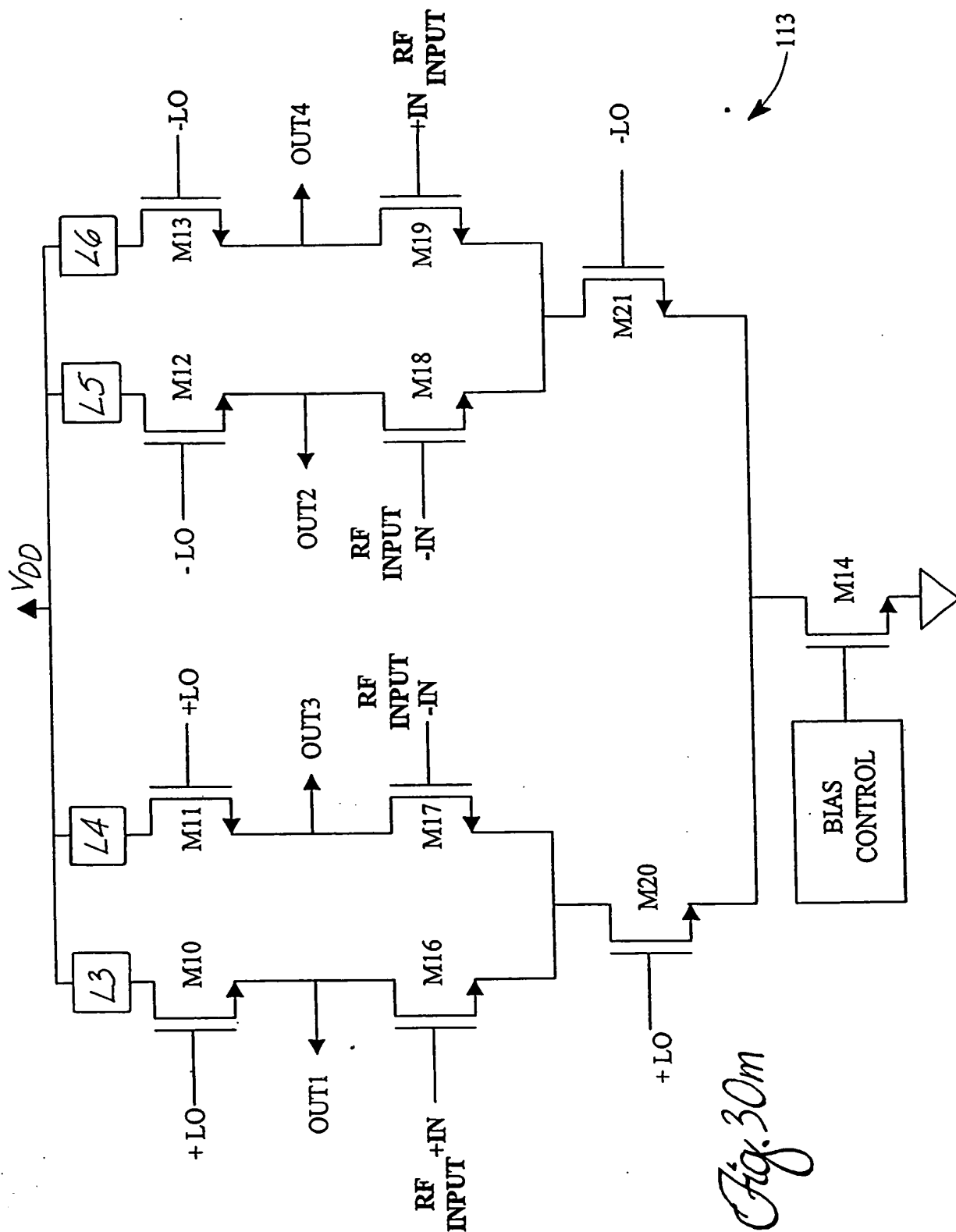


Fig. 30m

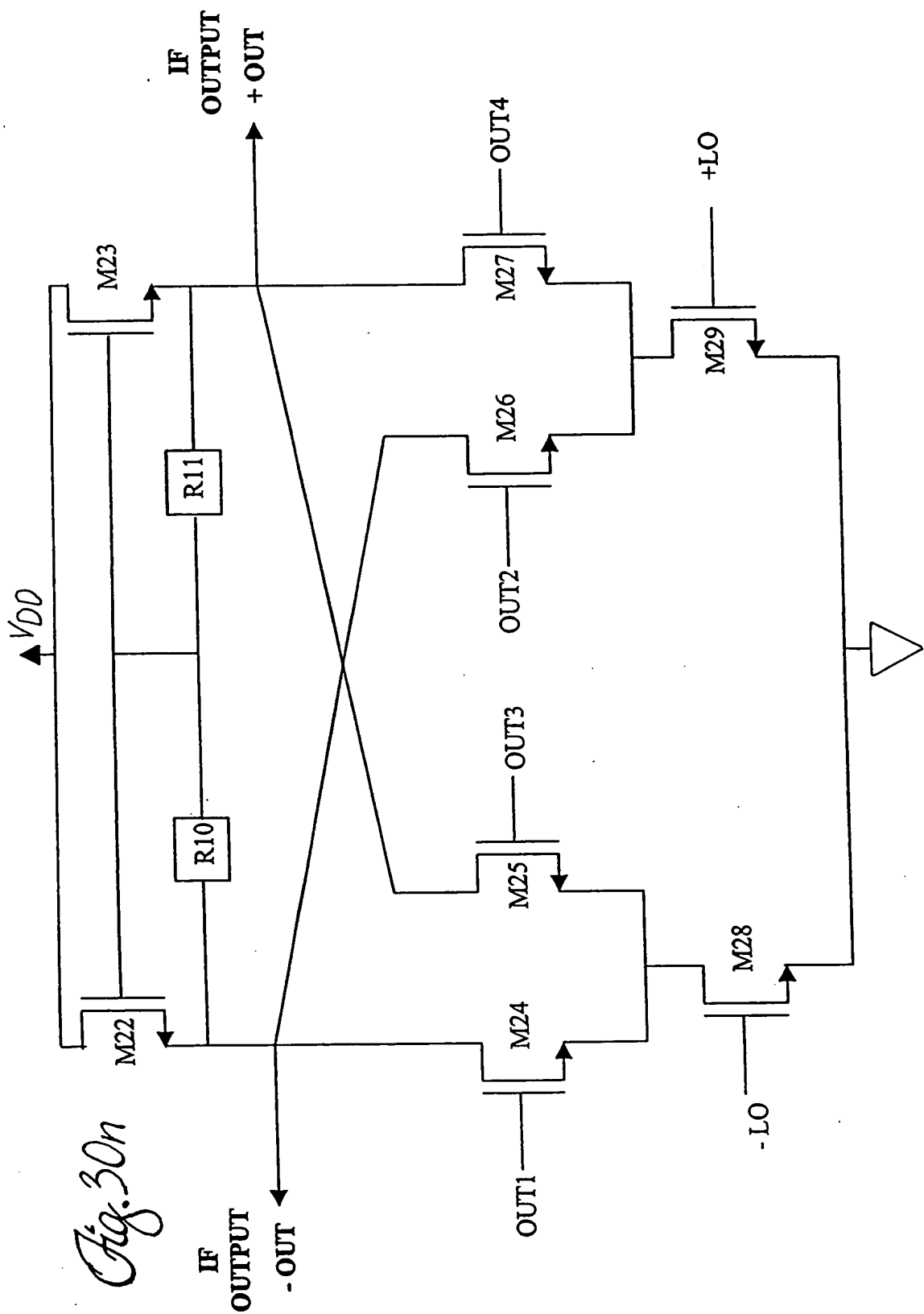


FIG. 31a

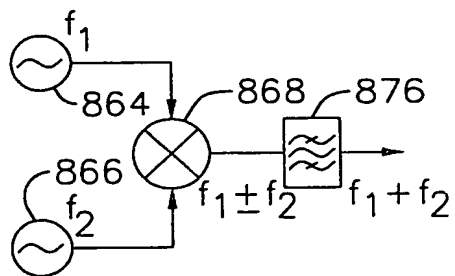


FIG. 31b

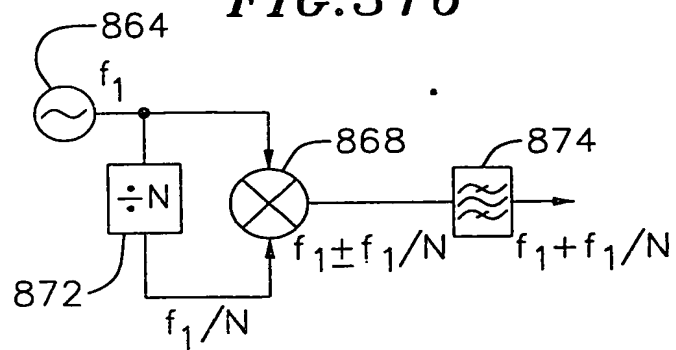


FIG. 32

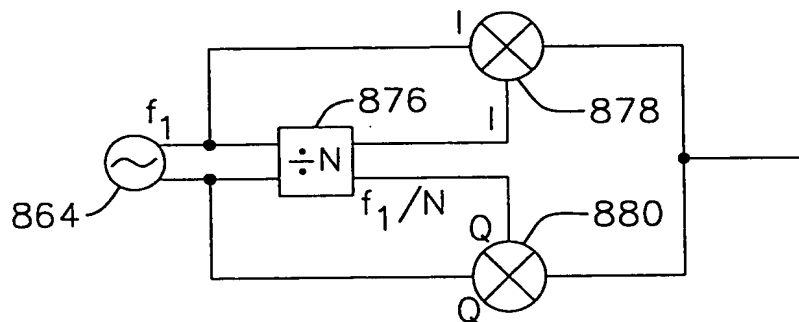


FIG. 33

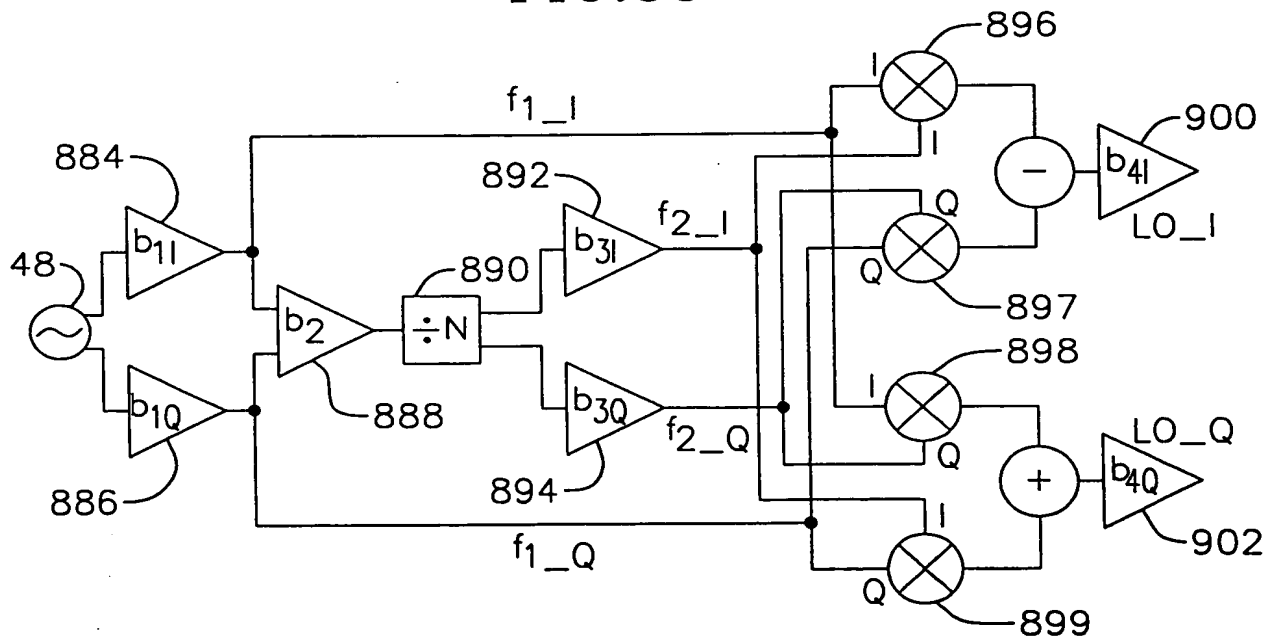


FIG. 33b

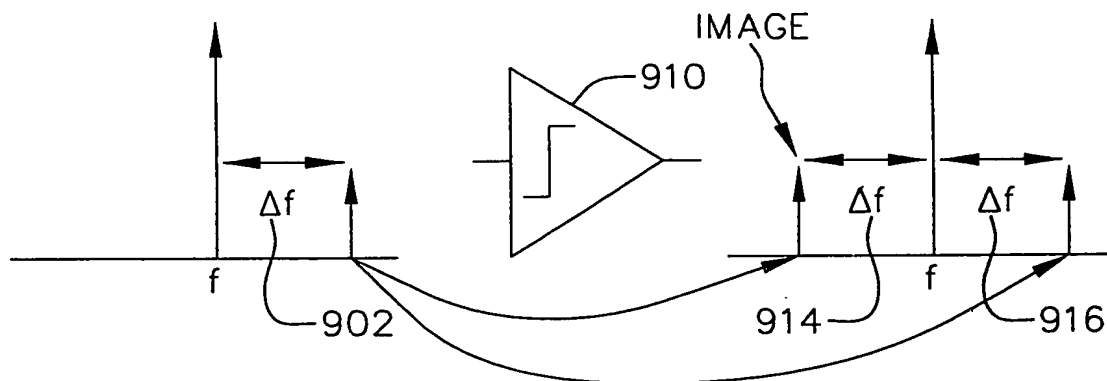


FIG. 34

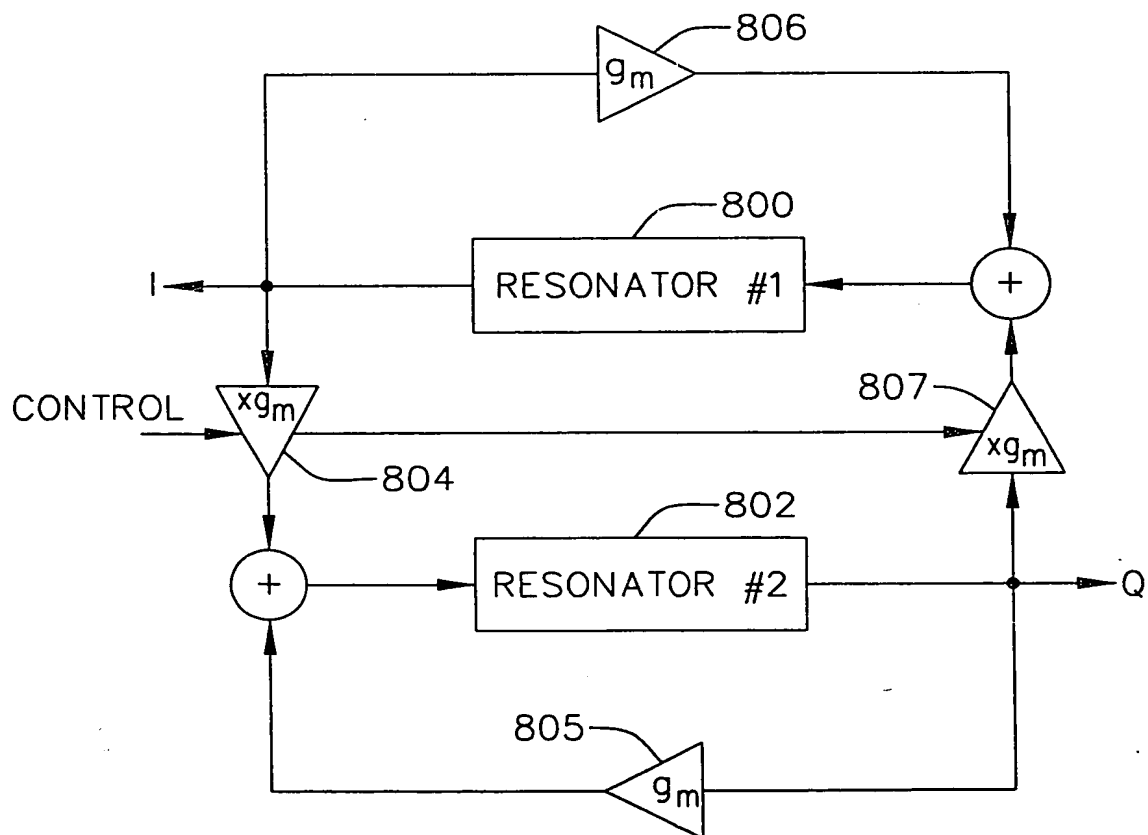
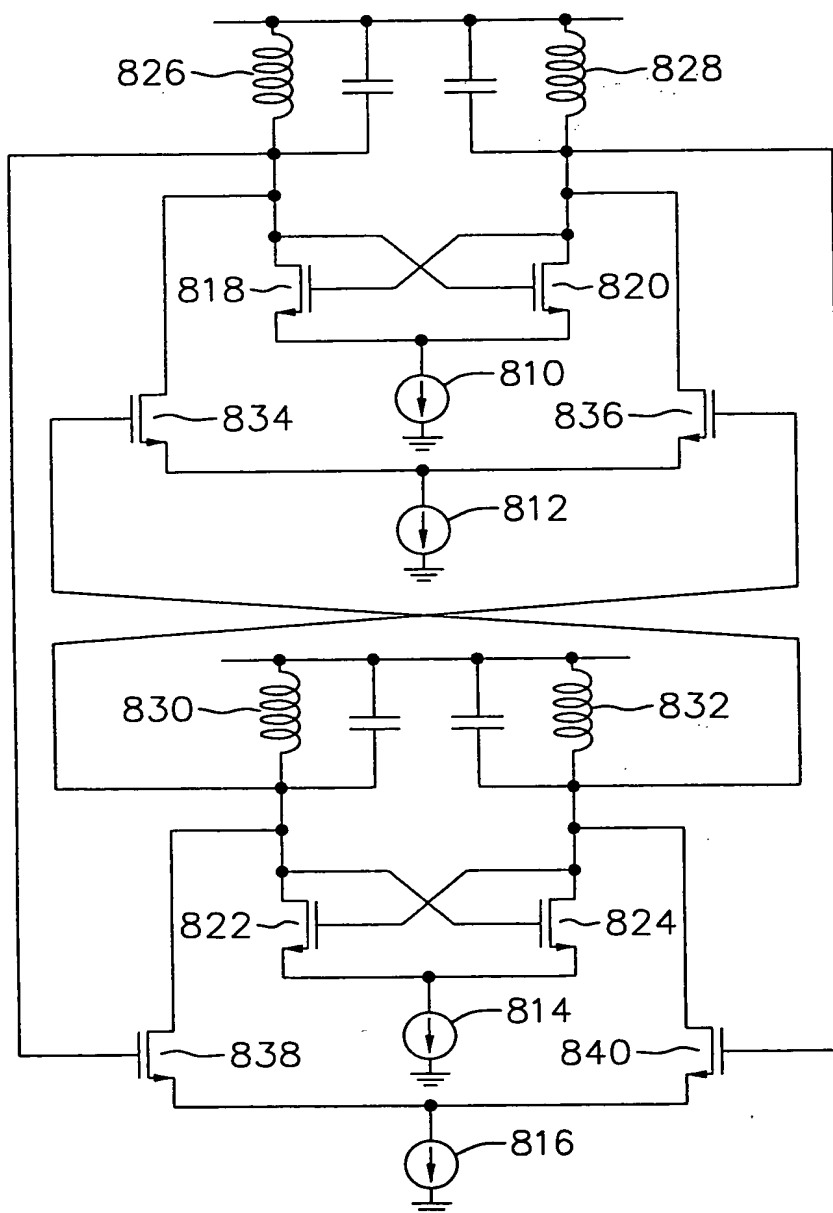
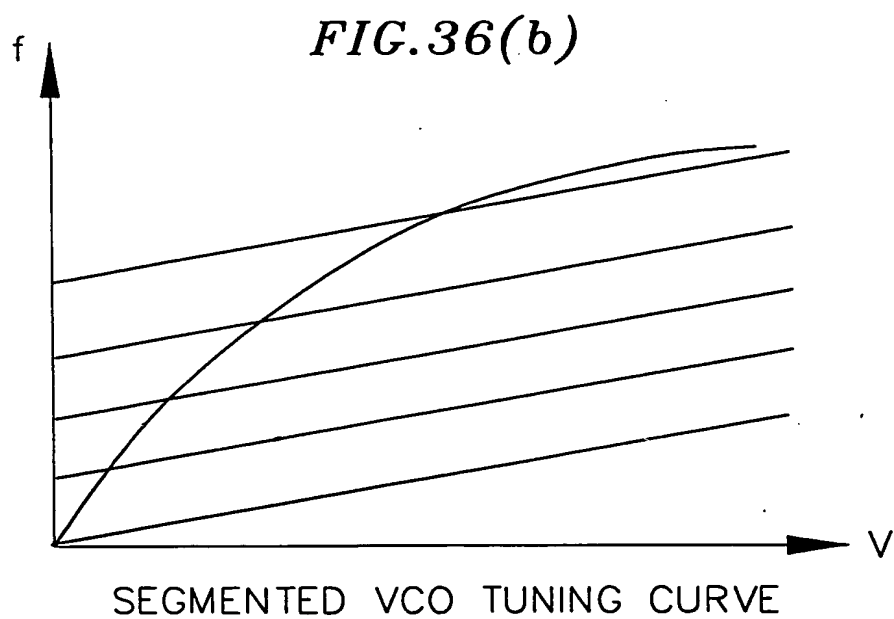
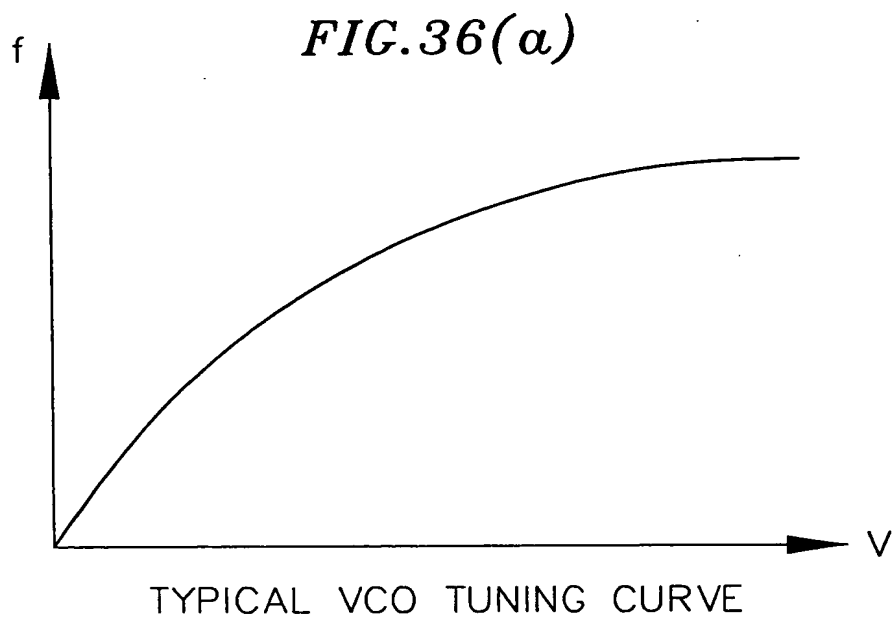


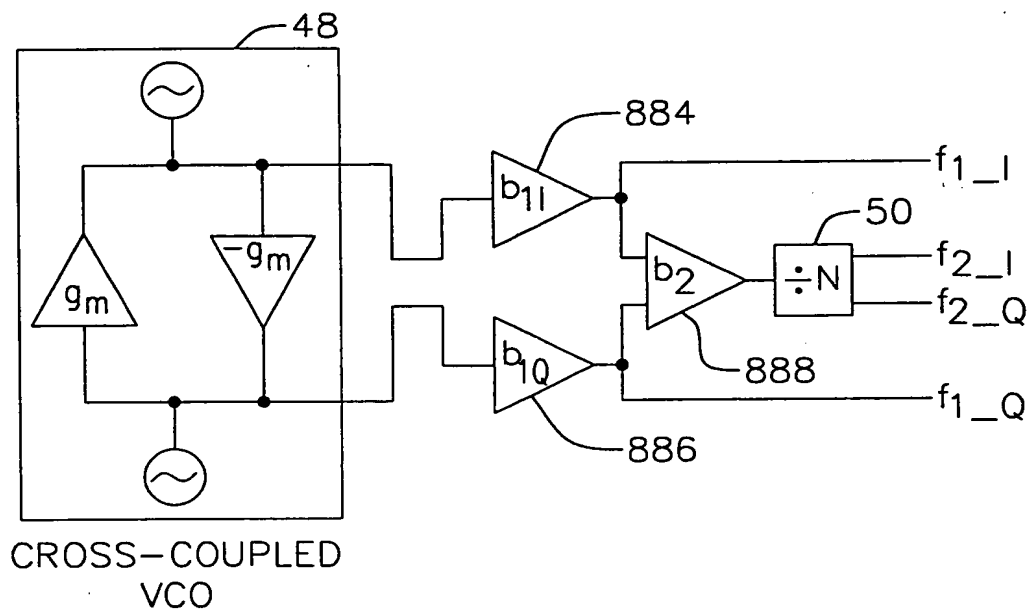
FIG. 35



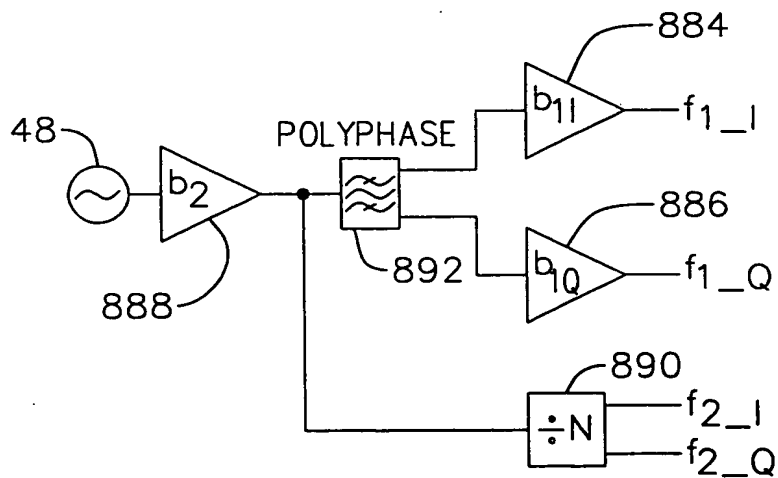




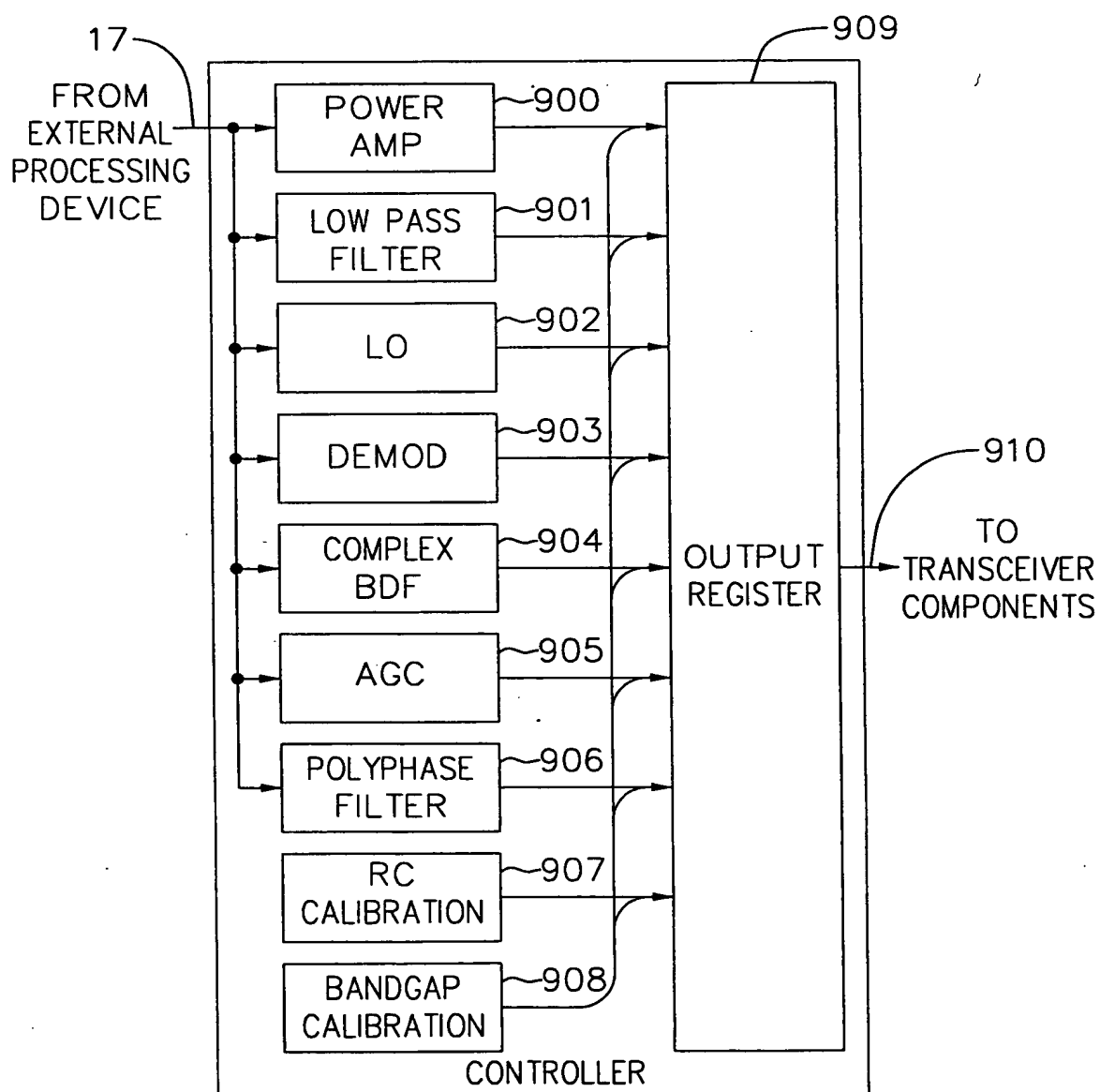
*FIG. 37a*

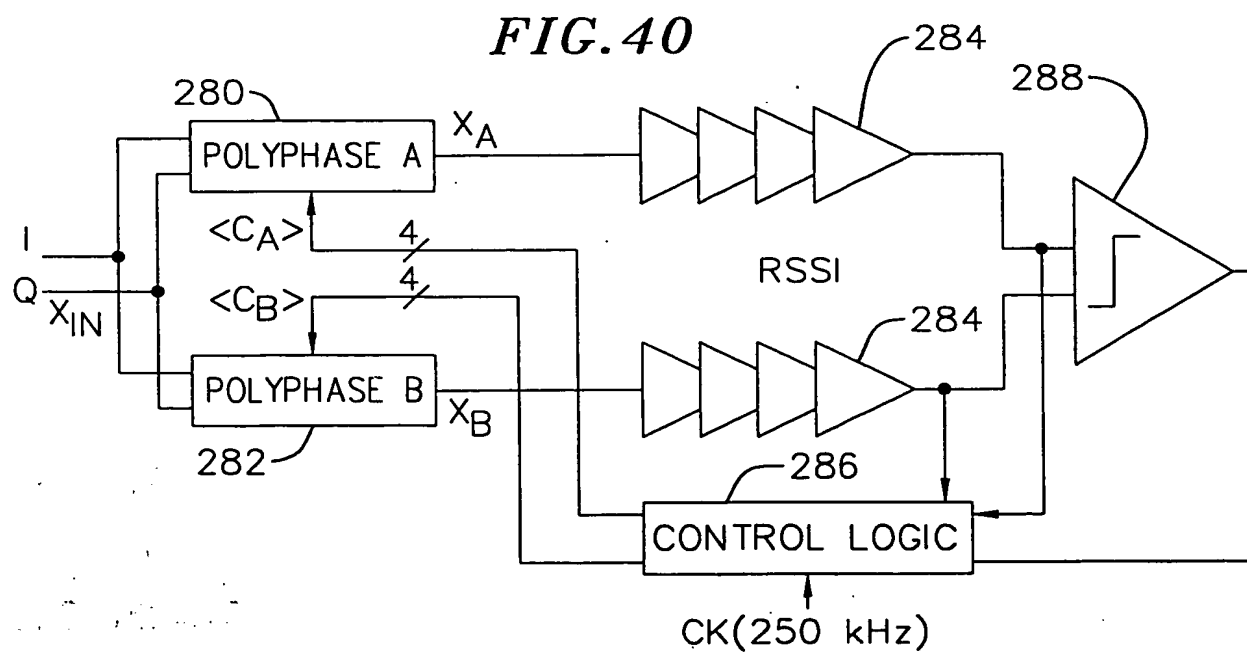
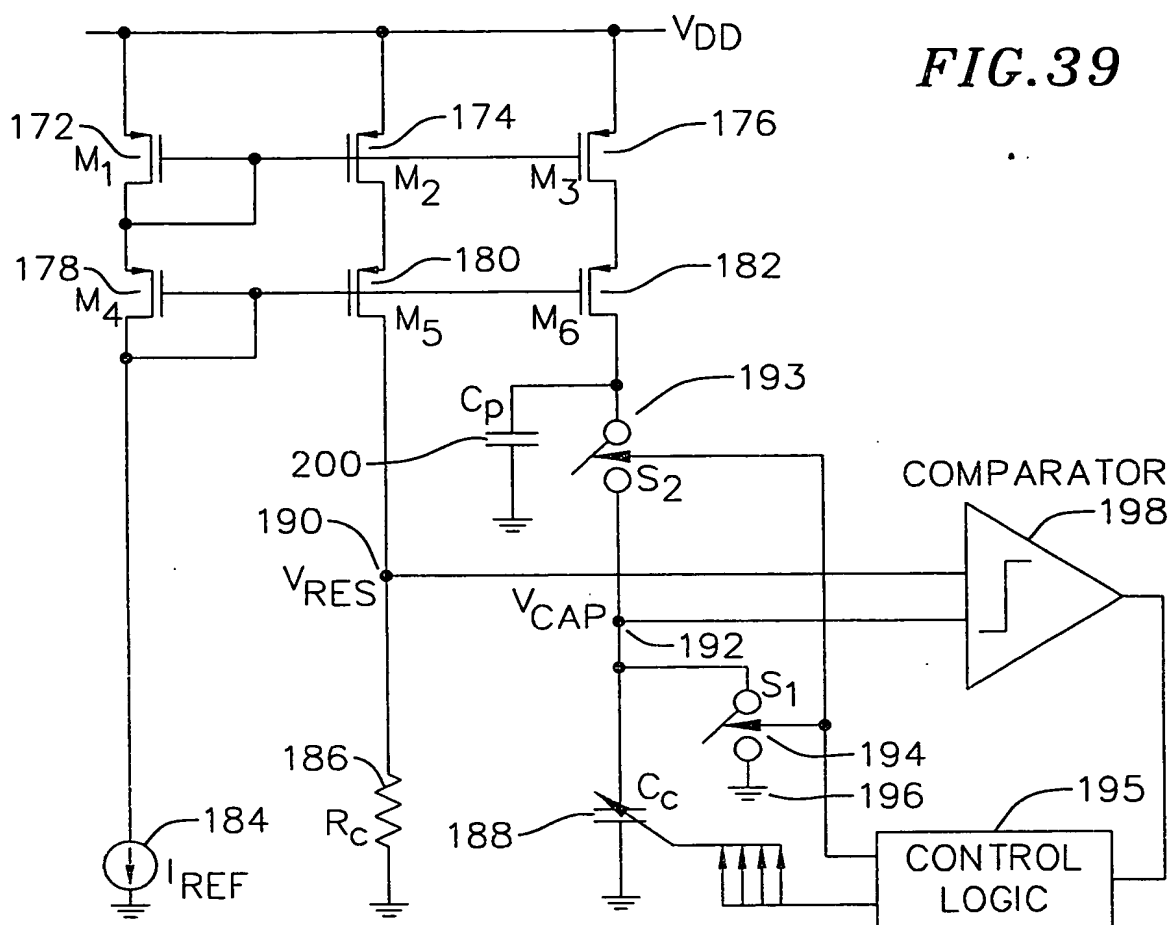


*FIG. 37b*

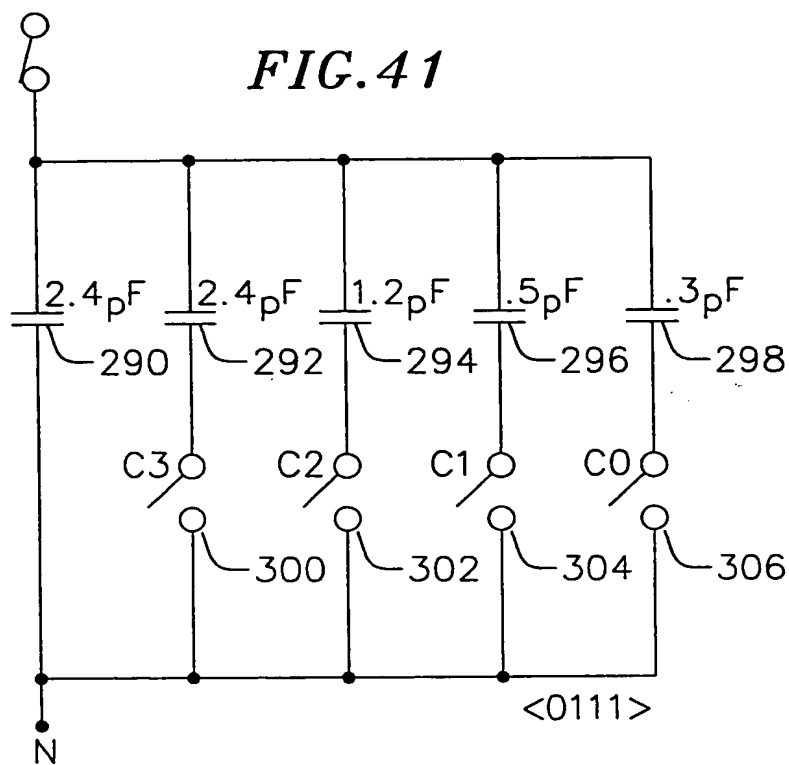


*FIG.38*





**FIG. 41**



**FIG. 42**

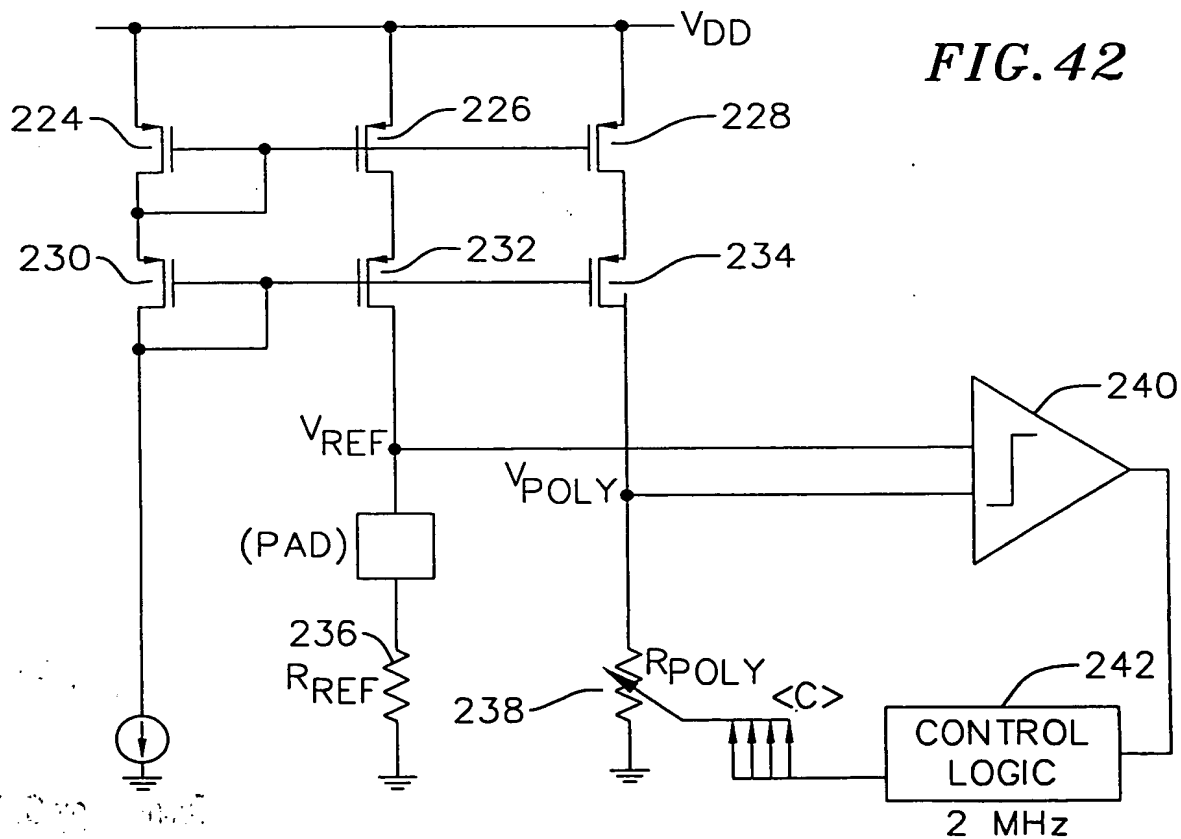


FIG. 43

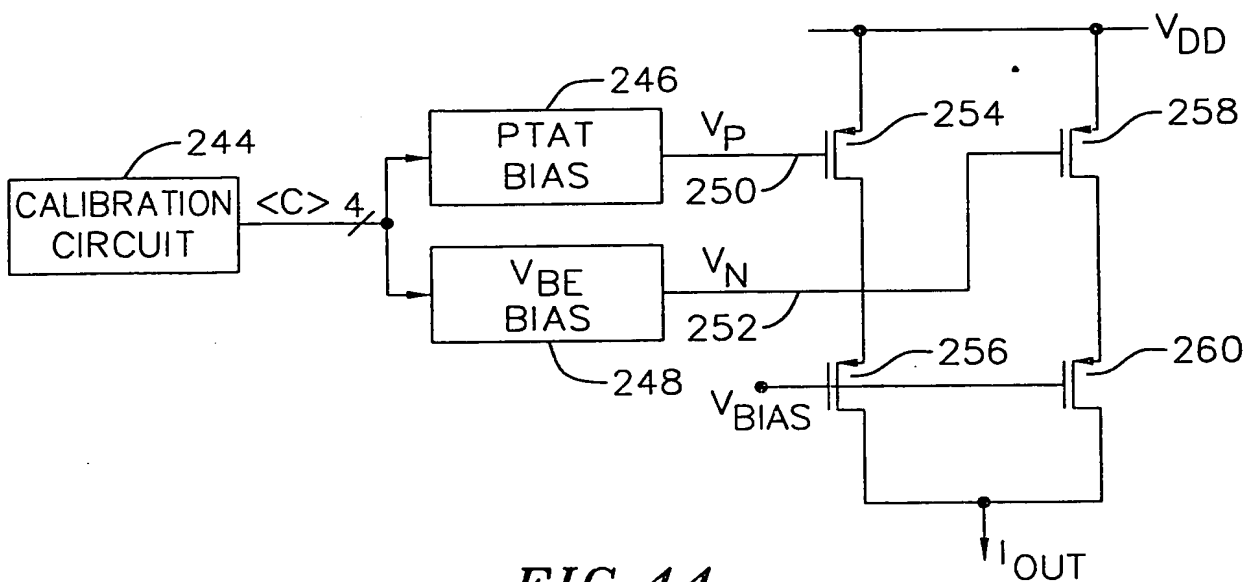


FIG. 44

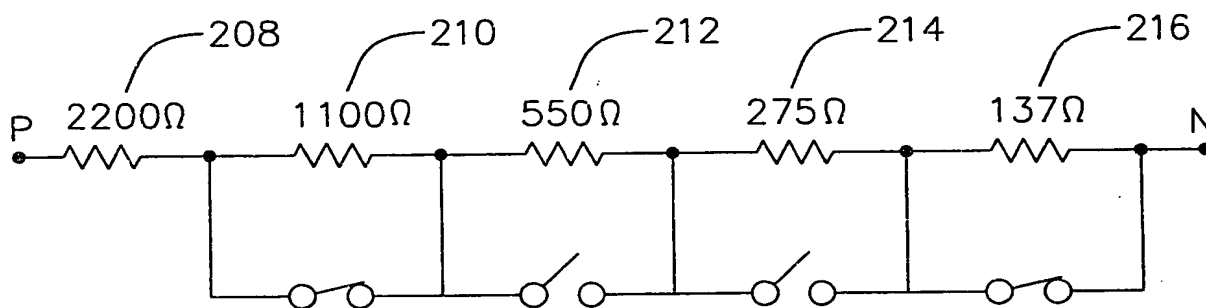
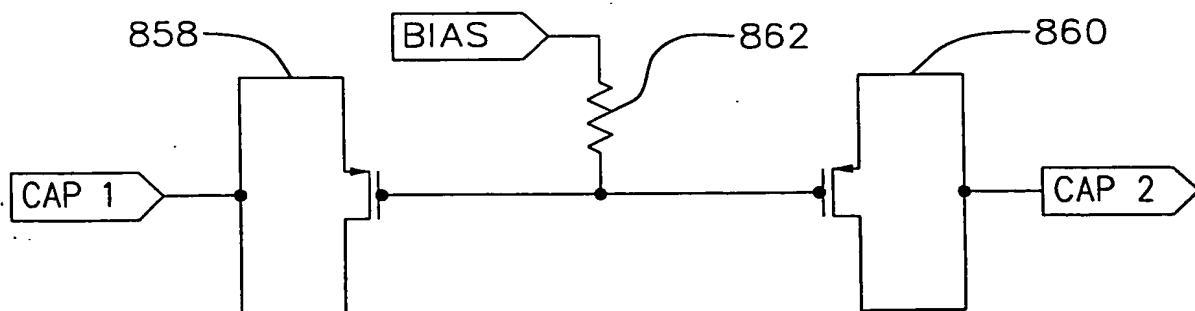
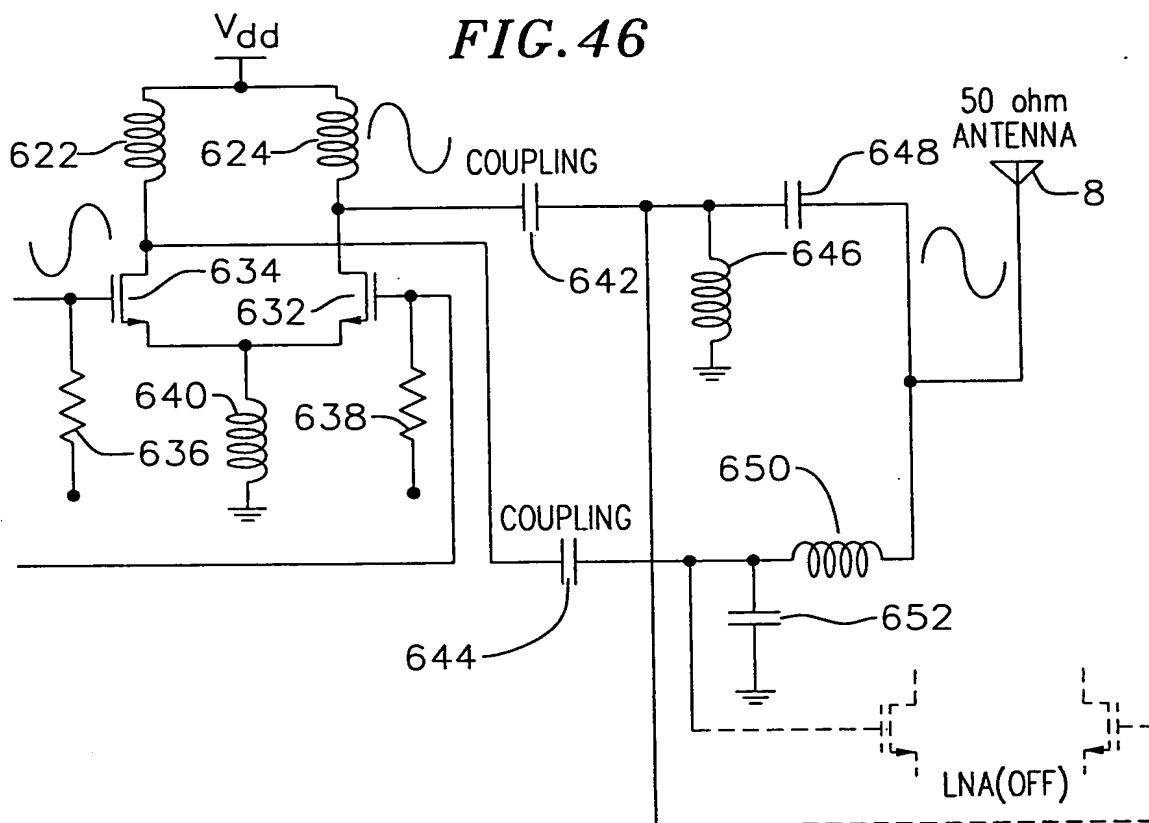


FIG. 45



**FIG. 46**



**FIG. 47**

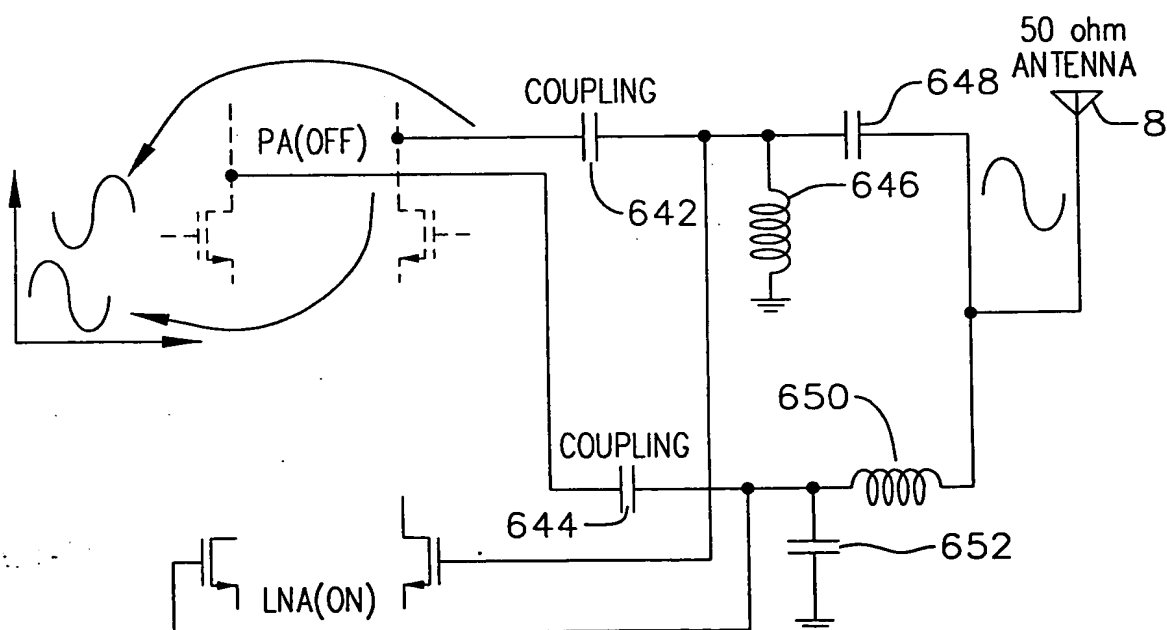
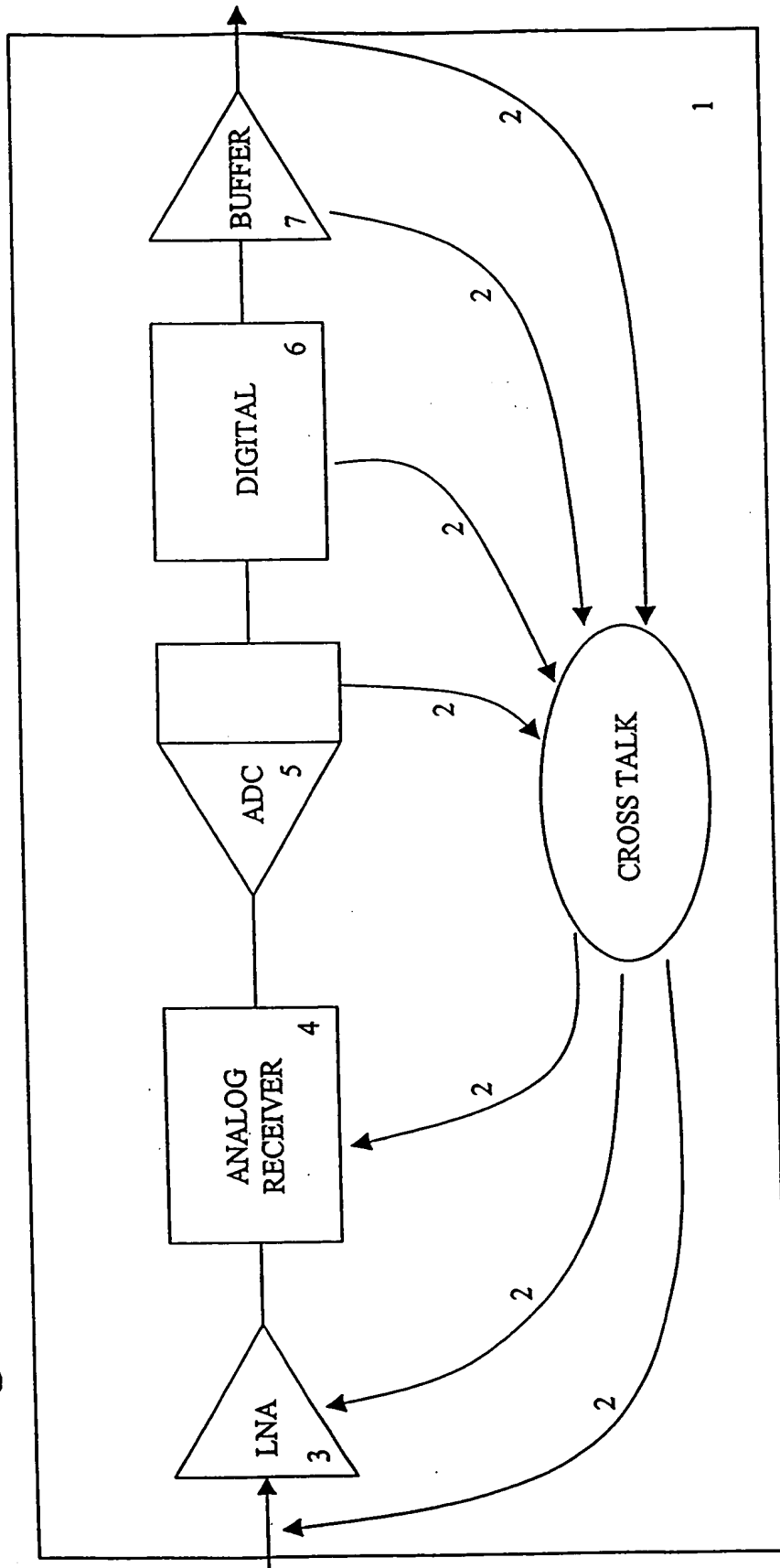
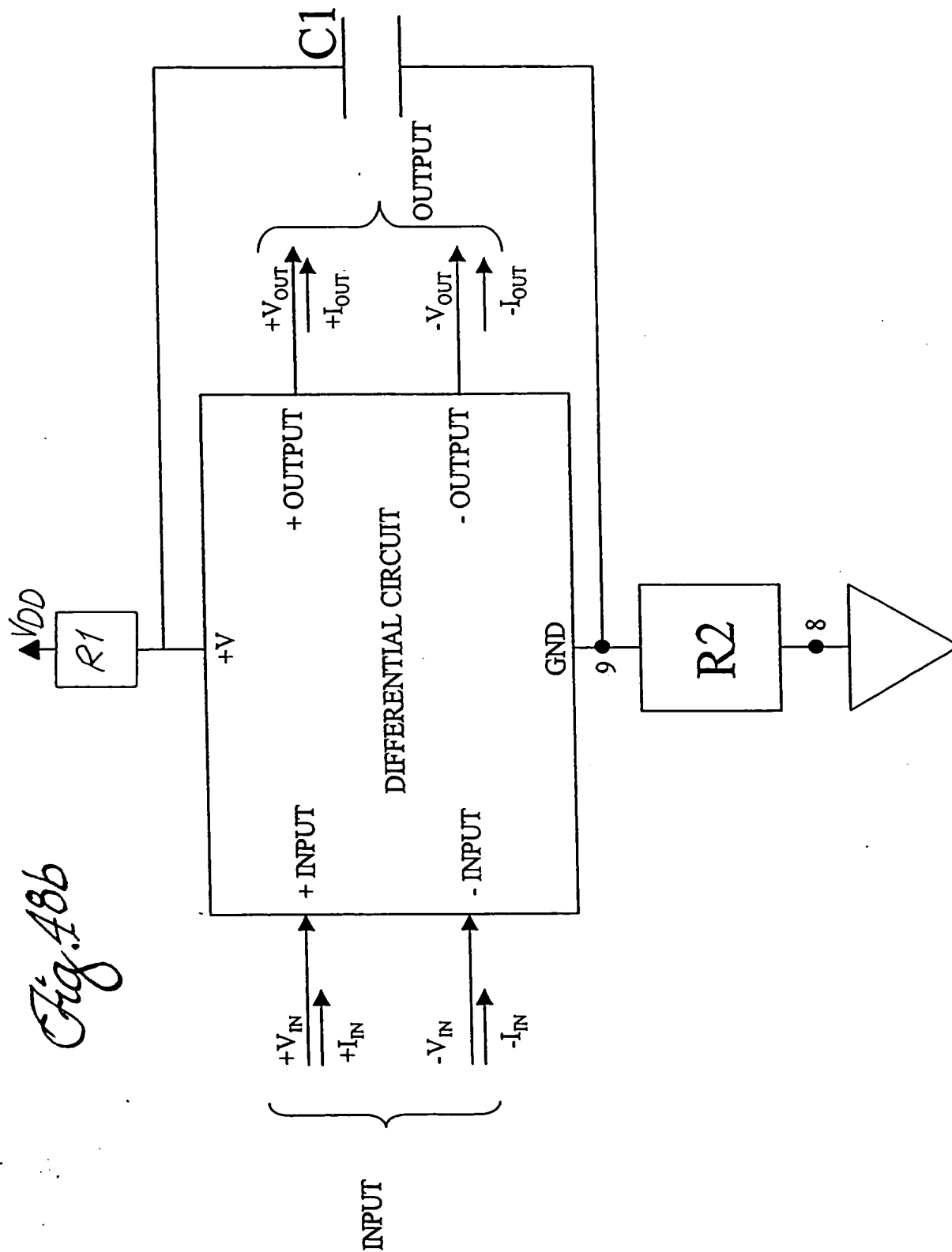
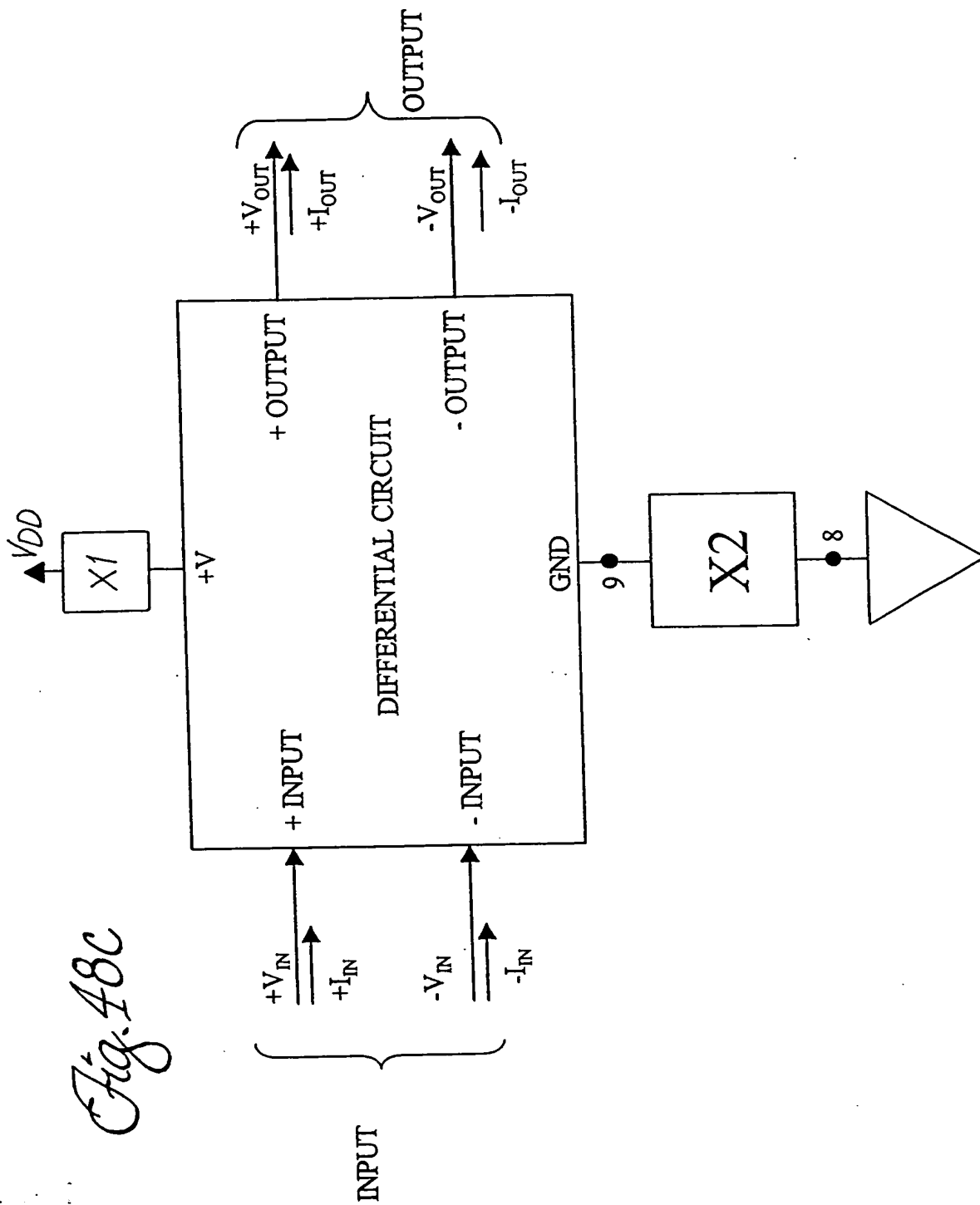


Fig. 48a









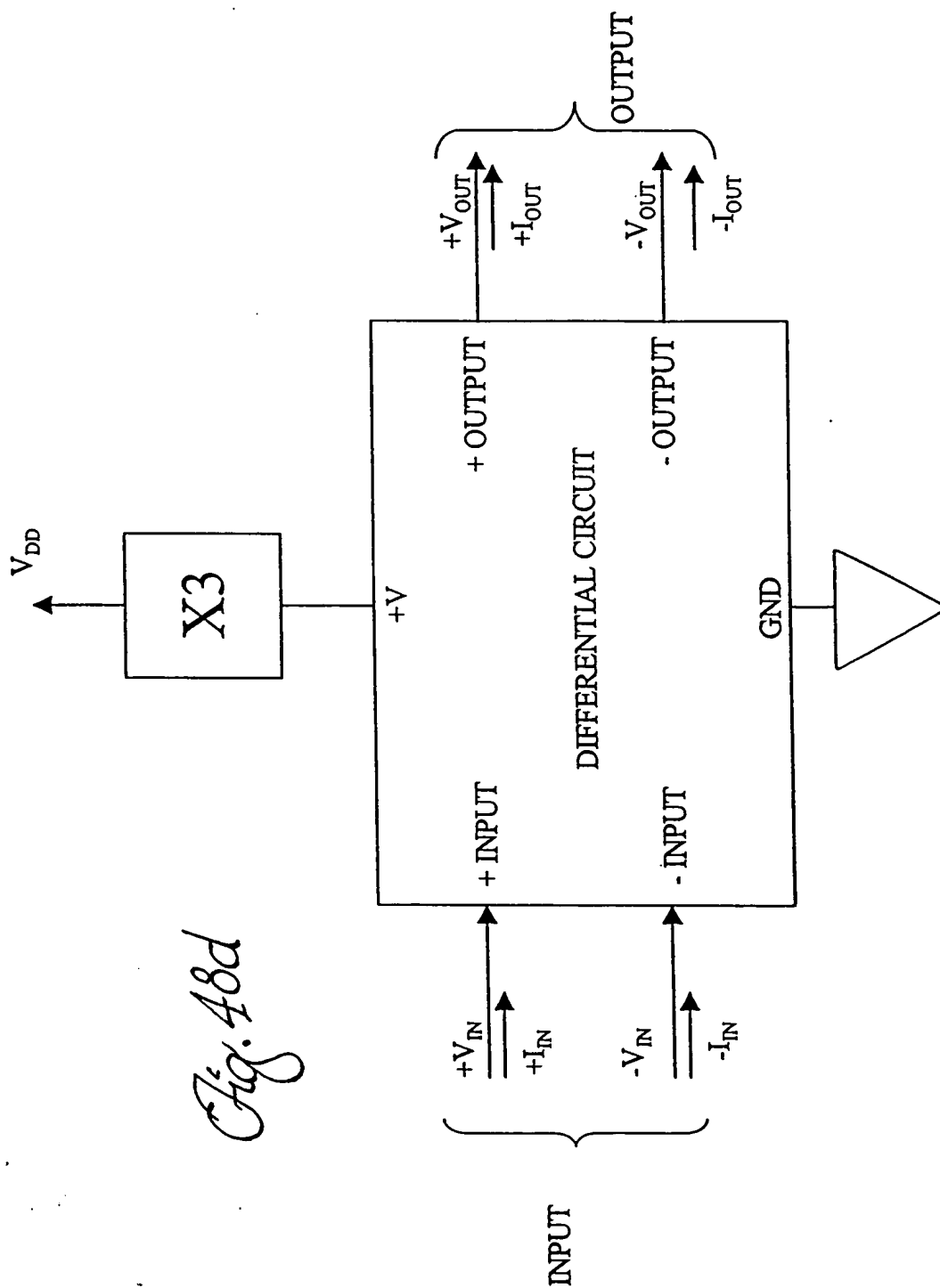
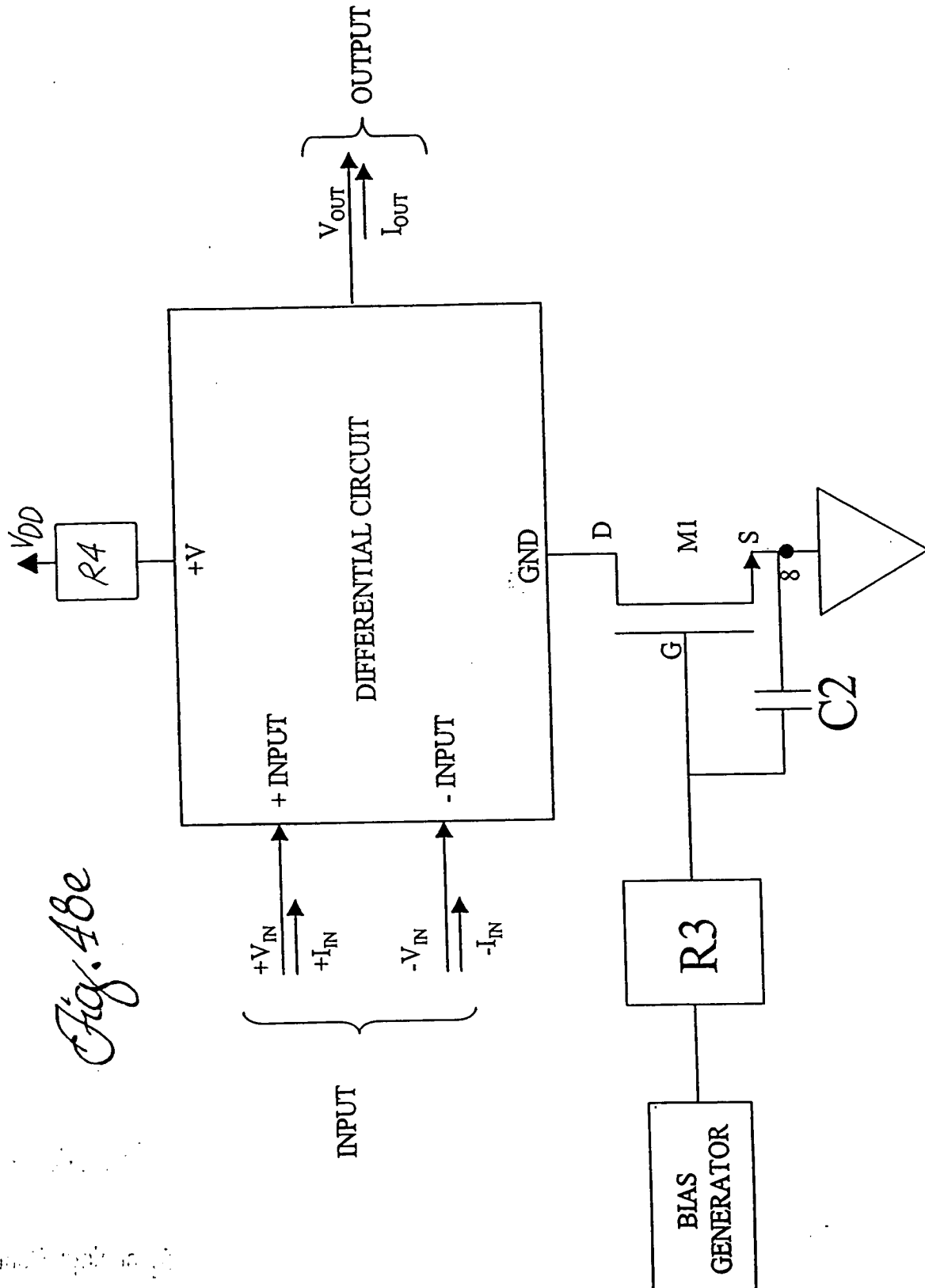


Fig. 48e



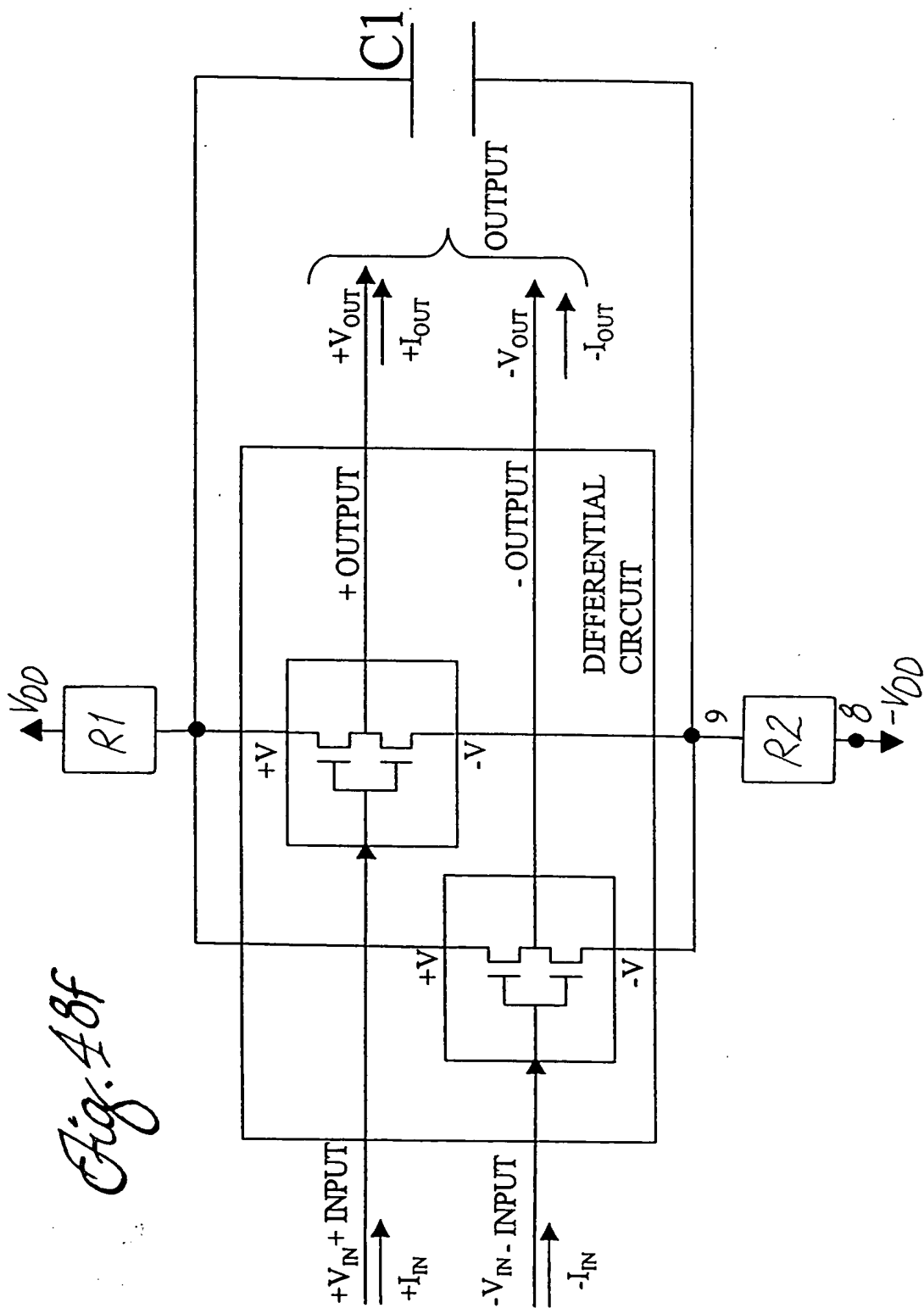


Fig. 48f